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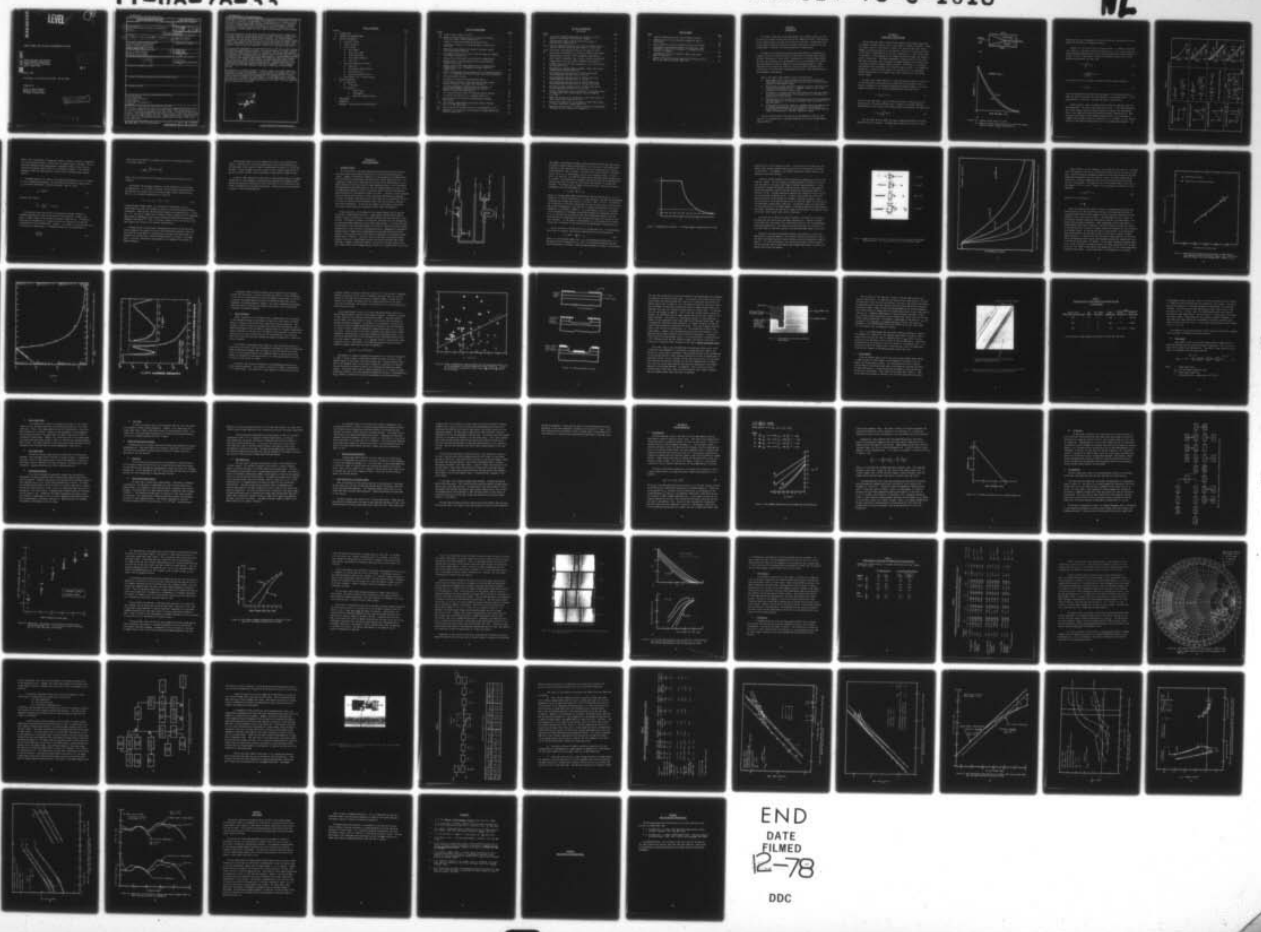

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GRADED CHANNEL FETs FOR NAVY ELECTROMAGNETIC SYSTEMS

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75222

August 1978

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This report summarizes the results of a program for development and evaluation of gallium arsenide field effect transistors (FETs) having graded doping profiles in the direction perpendicular to the surface. During the course of this program, such graded channel FETs were shown to be more linear than conventional FETs with flat channel doping profiles. Graded channel FETs are expected to be very beneficial for advanced microwave systems requiring highly linear solid state amplifiers.

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Included in the scope of the program was an analysis of the effects of graded profiles on linearity, the development and implementation of a method to grow epitaxial layers having graded profiles, fabrication and dc and rf characterization of graded channel FETs, development of a localized anodic oxidation procedure to utilize n^{+} contact layers, and an objective comparison of the properties of graded channel FETs with those of conventional, uniformly doped structures.

Theoretical analysis of the effect of nonuniform doping profiles showed that improved linearity is expected for profiles in which the doping concentration is greater near the active channel/buffer interface. For a given channel thickness and total doping concentration, the device having the largest "charge moment" (the integral across the active layer of the product of doping concentration and distance from the surface) was predicted to be more linear. The improved linearity was also predicted to result in an improved noise figure.

Procedures were developed for the epitaxial growth of FET active layers having exponentially graded doping profiles. This was achieved in a simple, reliable, reproducible manner using a mixing cell technique. FET devices fabricated on such material exhibited more linear dc transfer characteristics than did uniformly doped devices. Graded channel FETs having gates $\geq 1\ \mu m$ also showed improved third-order intermodulation performance when tested at X-band under standard test conditions. Graded devices having $2\ \mu m$ gates exhibited improved noise figures when compared to uniformly doped devices. Wideband amplifiers using graded devices exhibited improved third-order intermodulation and improved AM-to-PM conversion when compared to amplifiers employing uniformly doped devices.

The capability of growing epitaxial n^{+} contact layers on uniformly doped and graded active layers was developed. To fully exploit this capability, a localized anodic thinning technique was developed that enabled the self-limiting anodic oxidation procedure to be applied only to the channel region, leaving n^{+} material in the source and drain regions. Devices fabricated in this manner had source-drain burnout voltages approximately 10 V greater than did comparison devices lacking the n^{+} material.

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SECTION I
INTRODUCTION

This report summarizes the accomplishments of a research program carried out during a two-year period under Contract No. N00014-76-C-1016. The objective of this program was to evaluate the influence of non-flat or graded doping profiles within the channels of gallium arsenide field effect transistors on the maximum power, linearity, and noise properties of these devices.

Included in the scope of the program were development of procedures for growth, fabrication, and optimization of GaAs FETs with graded channel doping profiles, evaluation of the dc and rf characteristics of these graded channel devices, and comparison with the characteristics of conventional flat profile FETs fabricated with similar geometries and processing procedures. These characteristics included the linearity of the dc transfer characteristics (uniform g_m), the third-order intermodulation products, noise characteristics, and S-parameter measurements.

Some of the major accomplishments under the program were:

- Establishment of a simple, reliable, and reproducible process for vapor phase growth of epitaxial FET structures with controlled doping gradients in the channel regions.
- Modification of anodic oxidation procedures to permit localized, self-limited thickness reduction of the channel regions of FETs in the presence of n^+ epitaxial contact layers.
- Development of an analytical model that explains the improved linearity resulting from modifications of the doping profile in the direction perpendicular to the surface.
- Demonstration of an inverse relation between third-order intermodulation and gate length when the devices are operated under a standard set of test conditions.
- Demonstration of improved linearity, assessed both by the shape of the dc transfer characteristic and by third-order intermodulation, in graded channel FETs that have gate lengths of 1 μm or greater and are tuned for maximum gain in the gain compression region.

The next section details the theoretical considerations that form the basis for our expectations of improved properties of FETs with graded channel doping profiles.

SECTION II
THEORETICAL CONSIDERATIONS

The earliest FET model, the well-known gradual channel approximation due to Shockley, assumes that the ratio of gate length to channel thickness is large. This model, which is illustrated in Figure 1(a), predicts that even radical changes in the doping profile in the direction normal to the surface will have little effect on the shape of the transfer characteristic. This is discussed in Reference 1, and an example of this shape variation for power law doping is given in Figure 1(b). The modest dependence on doping profile is due to the fact that the channel under the gate is narrowed gradually from the drain end to the source end as the gate voltage increases. The effect is to modulate the doping profile more effectively laterally than vertically. For modern FET dimensions, in which the gate length is of the order of 1 μm, the gradual channel approximation is not appropriate unless combined with a saturated velocity model.

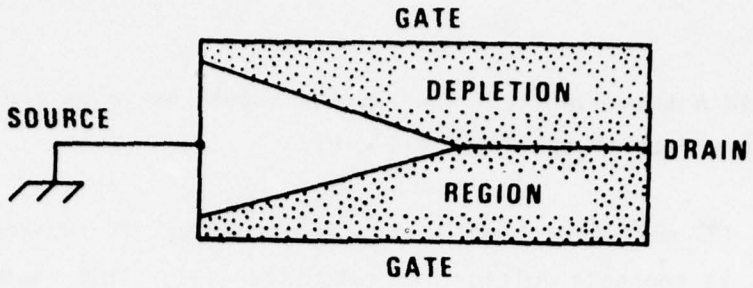
We shall use a simple depletion or saturated velocity model in which full current saturation is assumed under the gate and this saturated current is directly modulated by the difference between the depletion depth, w, and the channel thickness a. For uniformly doped material this model yields

$$I = qv_{sat}Z(a-w)N_o \tag{1}$$

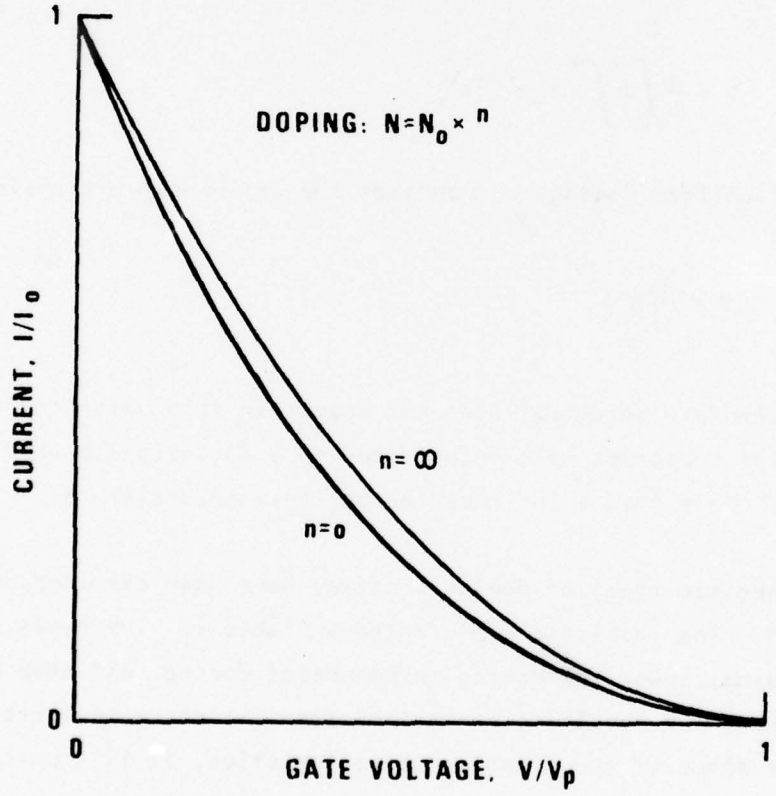
where Z is the gate width, v_{sat} the saturation velocity, and N_o the carrier concentration. For other profiles, N(x), in which x is distance measured perpendicular to the surface and increases toward the interface, the model gives

$$I = qv_{sat}Z\int_w^a N(x)dx \quad . \tag{2}$$

This saturated velocity model was used to examine the effect of various doping profiles on linearity. Although exact quantitative results of such



(a)



(b)

Figure 1(a) Gradual Channel Model of an FET.

(b) Range of Transfer Characteristics for Power Law Doping Using the Gradual Channel Approximation.

modeling should not be expected, the results should serve as qualitative indications of the effect of different profiles.

Equation (2) will give I(w) for a given profile. It remains to determine w(V), where V is the gate voltage, to calculate I(V). This is done using the simple depletion approximation in which the one-dimensional Poisson equation is solved. If E(x) is the electric field in the depletion zone, and V is the potential drop across this zone, then

$$-V = \int_0^w E(x)dx \tag{3}$$

$$V = \frac{q}{\epsilon}\int_0^w dx \int_x^w N(x')dx' \quad . \tag{4}$$

For the case of uniform doping, one obtains the well-known expression

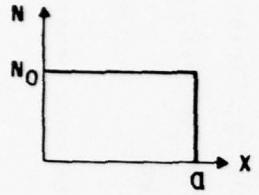
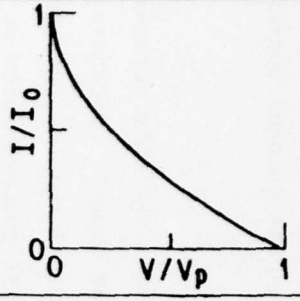
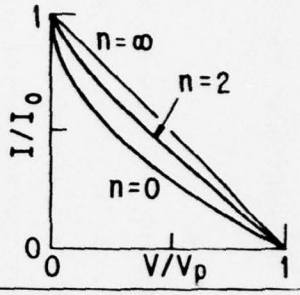
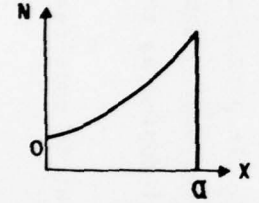
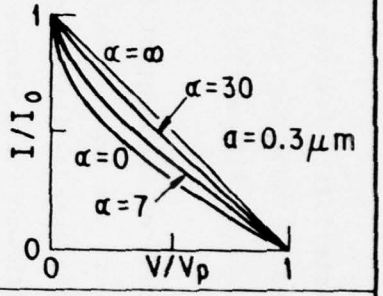
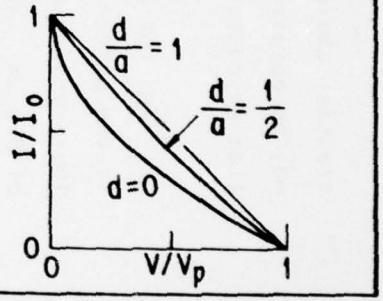
$$V = \frac{q}{2\epsilon} N_o w^2 \quad . \tag{5}$$

Since the source-drain potential does not appear in this saturated velocity model, no special subscript will be attached to V to designate that it is the gate potential. Note that V includes the built-in potential, ϕ.

Several specific types of doping profiles have been examined using the above equations. The results are presented in Table 1. The types considered are uniform doping, power law doping, exponential doping, and step doping. Table 1 also shows the resulting normalized transfer characteristics. When considering the shape of the transfer characteristics, it is important to remember that because the built-in potential, ϕ, is included in V, the initial portion of the transfer characteristic will not be externally apparent. The

Table 1

Transfer Characteristics For Various Doping Profiles

UNIFORM DOPING, $N=N_0$ 	$V = \frac{q}{2\epsilon} N_0 W^2$ $I = I_0 \left[1 - \left(\frac{V}{V_p}\right)^{1/2}\right]$	
POWER LAW DOPING, $N=N_0 x^n$ 	$V = \frac{q}{\epsilon} \frac{N_0}{n+2} W^{n+2}$ $I = I_0 \left[1 - \left(\frac{V}{V_p}\right)^{\frac{n+1}{n+2}}\right]$	
EXPONENTIAL DOPING, $N=N_0 e^{\alpha x}$ 	$V = \frac{q}{\epsilon} \frac{N_0}{\alpha^2} \left[1 - e^{\alpha W}(1-\alpha W)\right]$ I = No Analytic Expression in V/V_p	
STEP DOPING, $N = \begin{cases} N_1 & x < d \\ N_2 & d \le x \le a \end{cases}$ 	$W \ge d$ $V = \frac{q}{2\epsilon} N_2 \left[W^2 - (1 - \frac{N_1}{N_2}) d^2\right]$ $I = I_0 \left[1 - \frac{\left(1 + \left(\frac{a^2}{d^2} - 1\right)\frac{V}{V_p}\right)^{1/2} - 1}{\frac{a}{d} - 1}\right]_{N_1=0}$	

transfer characteristics for the case of power law doping contained in Table I may be compared to those for power law doping in the gradual channel approximation as contained in Figure 1(b).

For the case of exponential doping, the dimensionless variable parameter is the product of the exponential coefficient α, and the channel thickness, a. The transfer characteristics are plotted assuming a typical channel thickness of 0.3 μm. Although the presence of transcendental equations prohibits an analytic expression of I(V) for this case, a simple numerical calculation produces the transfer characteristics.

The final case in the chart is for "step doping" in which a lightly doped layer of carrier concentration N_1 overlays a more heavily doped layer of carrier concentration N_2. It is assumed that the values of N_1 and d are such that the built-in potential ϕ entirely depletes the N_1 layer. In these calculations the doping level N_1 always appears in the combination

$$\left(1 - \frac{N_1}{N_2}\right) ,$$

and hence for $N_2 \geq 10\ N_1$, N_1 can be assumed equal to zero with little error in further calculations.

All three types of nonuniform doping achieve exact linearity as the appropriate variable parameter is taken to its limit (Table I). Note that both power law and step doping appear to approach linearity more "quickly" than does exponential doping as the relevant parameter is varied.

It is useful to consider the effect of doping profiles more generally.

To this end, Equation (4) may be rewritten in another form by partially integrating on Equation (3):

$$-V = xE(x)\Big|_0^w - \int_0^w xE'(x)dx \tag{6}$$

$$V = \frac{q}{\varepsilon}\int_0^w xN(x)dx \quad . \tag{7}$$

Thus, the depletion voltage is proportional to what may be called the charge moment--the integral of the product of the amount of charge and its distance from the surface. It follows that the pinchoff voltage is given by

$$V_p = \frac{q}{\varepsilon}\int_0^a xN(x)dx \quad . \tag{8}$$

Equations (2) and (7) imply

$$\frac{dI}{dw} = qv_{sat}ZN(w) \tag{9a}$$

$$\frac{dV}{dw} = \frac{q}{\varepsilon}\,wN(w) \quad . \tag{9b}$$

Thus,

$$g_m = \frac{dI}{dV} = v_{sat}Z\varepsilon\,\frac{1}{w(V)} \quad . \tag{10}$$

Thus, linearity (constant g_m) is approached by those profiles in which the depletion depth w, changes very little as a function of gate voltage, V. That is, dw/dV should be small, or by Equation (9b) the product wN(w) should be large.

Hence, for a fixed amount of charge and channel thickness, linearity is approached as the available charge is placed near the channel-buffer interface. This is why power doping and step doping appear to approach linearity more "quickly" than does exponental doping (Table 1) for moderate increases in the relevant parameter--power and step doping do a better job of producing higher charge moments.

Although Equation (10) implies a decreased transconductance, g_m, as a result of this increased charge moment, the more important ac quantity, g_m/C_g, where C_g is the gate capacitance, remains unaffected. That is, since

$$C_g = \frac{\varepsilon(\text{Area})}{w} \quad , \tag{11}$$

Equation (10) implies

$$\frac{g_m}{C_g} = \frac{v_{sat}\, Z}{(\text{Area})} = \text{Constant.} \tag{12}$$

The modeling could be continued to calculate third-order products or sideband suppression for each of the specific profiles above. However, this amount of detail seems to be pushing a dc analytic model too far. In addition, other entities besides the I-V transfer function are involved in third-order intermodulation, as discussed below. However, it is useful to note that the ratio of third-order sideband power to fundamental power will be proportional to

$$\frac{d^3I}{dV^3} \Big/ \frac{dI}{dV} \quad , \tag{13}$$

which can be calculated for a general profile, N(x), and depletion depth, w, to be proportional to

$$\frac{1}{w^4 N^3(w)} \left[3N(w) + wN'(w) \right] \quad .$$

Hence, the first derivative of the doping profile also contributes to nonlinearity.

Nonlinearity at microwave frequency is often determined by third-order intermodulation. It is useful to consider the third-order intermodulation as arising from two sources, the first being the gate transfer characteristic. That is, for a transfer characteristic of the form

$$I = a_o + a_1 V_g + a_2 V_g^2 + a_3 V_g^3 + \ldots \quad , \tag{14}$$

an applied gate voltage signal, V_g, consisting of frequencies f_1 and f_2 (and perhaps a dc bias) will produce an output current containing many product frequencies. These include the third-order products at frequencies $2f_2 - f_1$ and $2f_1 - f_2$. The use of a power series transfer function [Equation (14)] to generate these product frequencies is well known and has also been done assuming order-dependent time delays.[2,3] Thus, third-order products arise from the cubic term (and higher-order terms) of the transfer characteristic.

A second source of third-order intermodulation arises from the mixing of various products, principally the first- and second-order products, within the drain portion of the device.[2] Alternatively, the drain contribution can be thought of as arising from a transfer characteristic of its own.[2] This means that, in practice, third-order intermodulation will depend on the output impedance matching.

The improved linearity is also expected to result in an improved noise figure. Noise figure is inversely proportional to the transconductance g_m, and the lowest noise figure is usually obtained when the device is biased near pinchoff. Since a graded structure is better able to maintain good values of g_m near pinchoff, superior noise performance is expected for graded devices.

To verify these theoretical predictions of improved performance for graded channel FETs, it was necessary to develop the procedures for epitaxial growth and device fabrication required for such devices and to fully characterize the dc and rf properties of the resulting devices. These activities are discussed in detail in the following section.

SECTION III
DEVICE DEVELOPMENT

A. Epitaxial Growth

All field effect transistors examined during the course of this program were fabricated from epitaxial GaAs grown with the well-known $Ga/AsCl_3/H_2$ system. Emphasis was placed on comparison of the properties of graded channel FETs with those of conventional FETs having flat channel doping profiles. For a meaningful comparison it was essential to minimize the large number of variables associated with fabrication of these advanced devices. This requirement was approached by epitaxial growth of flat and graded channel structures using the same growth apparatus (often in successive growth runs) and simultaneous batch processing of the comparison wafers into FETs. Initially, single epitaxial layer structures grown directly on semi-insulating substrates were employed; but later, epitaxial, high resistivity buffer layers were incorporated into the structure to isolate the active channel layers from the relatively imperfect bulk substrate material. During the last phase of the program, three-layer structures incorporating an n^+ epitaxial contact layer were examined.

Proper evaluation of the effects of the channel doping profile requires slices with a wide range of profiles. These doping profiles should decline smoothly without interruption in a controlled manner from the substrate to the surface. Fortunately, a simple, but effective, method[4] exists for exponentially varying a gas phase composition during vapor phase epitaxy. A similar technique was employed to grow the graded channel structures by varying the ambient dopant concentration in the vicinity of the growing crystal. Exponentially decreasing concentrations of dopant were incorporated into the layer during the growth process. The principle may be illustrated by reference to the epitaxial growth scheme shown in Figure 2. Initially, prior to the start of epitaxial growth, selector value (S_1) is positioned to permit the flow of the lower gas stream (hydrogen + dopant) through the reservoir (V) and into the main reactor tube. This stream contains donor dopant species (sulfur) at a concentration (C_o) which,

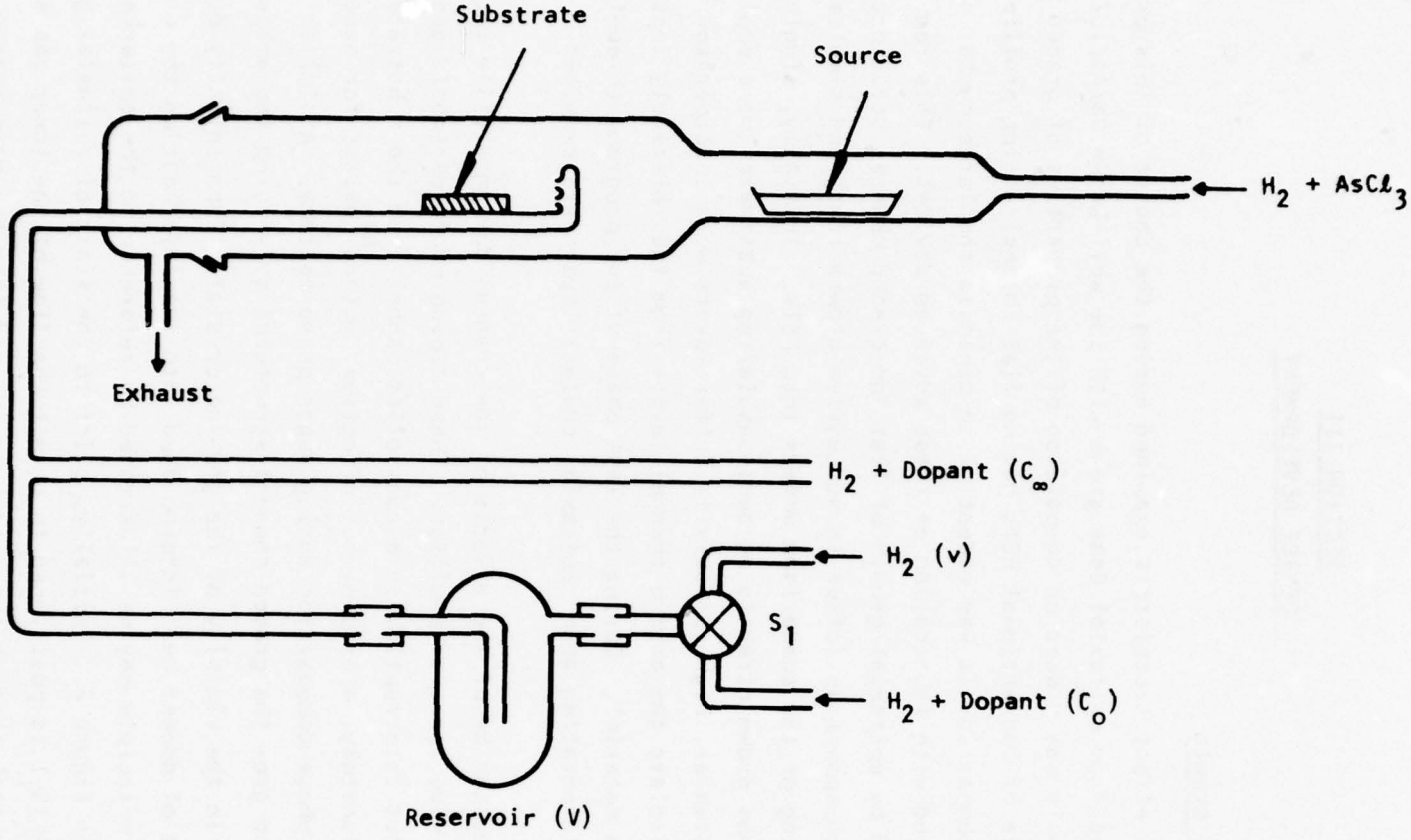


Figure 2 Scheme for Achieving Exponential Doping Profiles

when added to the background dopant supply and mixed with the main gas stream, provides an ambient dopant concentration in the vicinity of the substrate appropriate to that required for the desired carrier concentration at the substrate/epitaxial layer interface. Coincident with the initiation of epitaxial growth, valve S_1 is repositioned to admit a pure hydrogen stream. At this point, the reservoir is filled with a gas mixture having a dopant concentration, C_o; however, the concentration of dopant leaving the reservoir and passing over the growing crystal will decline with time as the reservoir is purged with hydrogen. The concentration of dopant entering the main reaction tube can be expressed by the following equation:

$$C = C_o \exp\left(-\frac{v}{V} t\right) + C_\infty \quad ,$$

where C is the gas phase dopant concentration entering the reactor; C_∞ is the background or minimum concentration; v is the volumetric flow rate of the hydrogen stream passing through the reservoir of volume, V; and t is time. (To simplify the illustration, corrections associated with the dilution effects of each hydrogen stream are neglected.) The variation in dopant concentration with time is graphically illustrated in Figure 3. At t_o the selector valve S_1 is switched to pure hydrogen, and the dopant concentration begins its exponential decline. If t_o is then made to coincide with the start of epitaxial growth, then the resulting carrier concentration within the epitaxial layer will decline as the layer thickens. If the growth is terminated at t_f, the surface carrier concentration will correspond to that produced by gas phase dopant concentration C_f.

Since, the carrier concentration (n) is proportional to C, if the epitaxial growth rate is constant, the resultant doping profile can be expressed by

$$n = n_o \exp\left(-\frac{v}{Vg} x\right) + n_\infty \quad , \qquad (15)$$

where g is the epitaxial growth rate, n_∞ is the background doping level, n_o is the doping level corresponding to C_o, and x is the distance measured from the substrate/epitaxial interface. Note that each parameter is known or can be easily

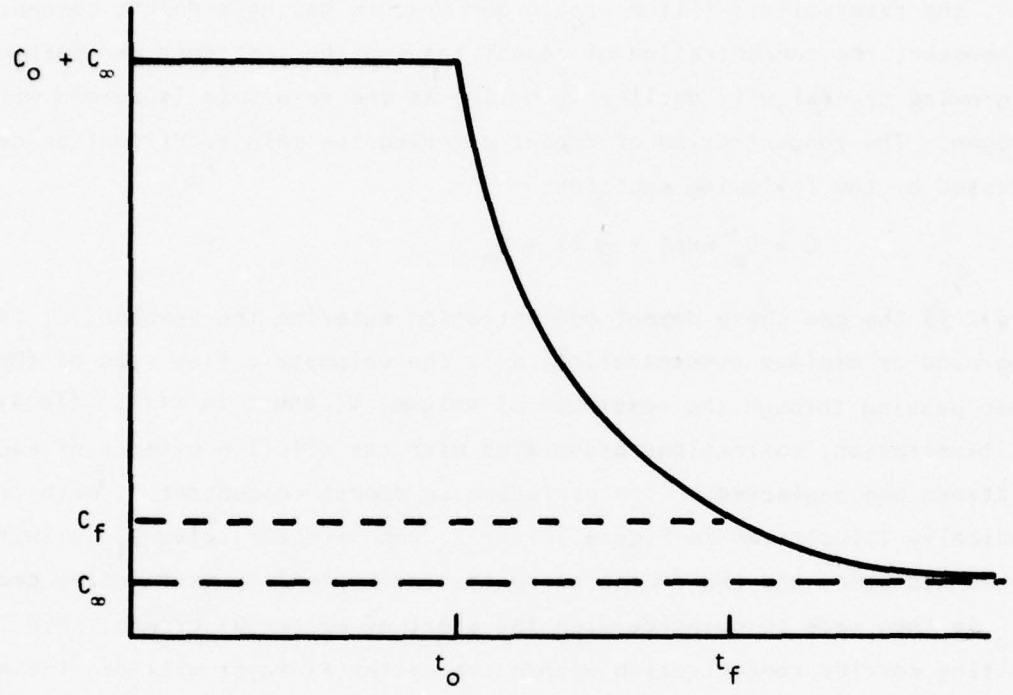


Figure 3 Hypothetical Variation in Gas Phase Dopant Concentration with Time

determined for a given epitaxial system. It should also be stressed that the doping levels decline smoothly and continuously from the substrate interface to the surface. The method is very simple and does not require complex time-dependent value manipulations.

Different channel gradients may be obtained by changing the volume of the reservoir vessel. For this purpose, the glass vessels illustrated in Figure 4 were fabricated to provide a wide range of channel doping gradients. To experimentally simulate the effects produced by the reservoirs, a gas analysis system was assembled to monitor the gas composition leaving each vessel as a function of time. The gas composition detector was a thermal conductivity cell utilizing matched thermistor pairs. Initially, each vessel was filled with helium containing a small amount of nitrogen to simulate the dopant; then a four-way selector valve was activated so as to flush the vessel with pure helium (minimum dopant concentration condition). The detector output is proportional to the concentration of nitrogen (dopant) in the gas stream leaving the reservoir and, hence, represents the variation in dopant concentration to be expected within the crystal growth region under similar conditions.

A typical set of results is shown in Figure 5. At point "A" the valve is switched, and the concentration decreases exponentially. Analysis of these curves shows that they agree within experimental accuracy with the dependences predicted theoretically. The smoothly varying compositions as a function of time were ideal for epitaxial growth of the desired graded channel structures.

Because of the excellent agreement between the simulation runs and the theoretically predicted behavior, the reservoir system was installed in one of the Texas Instruments epitaxial growth systems using the configuration shown in Figure 2. For rapid evaluation of the resulting profiles a mercury Schottky barrier probe was used to make capacitance-voltage measurements from which the doping profile could be deduced.

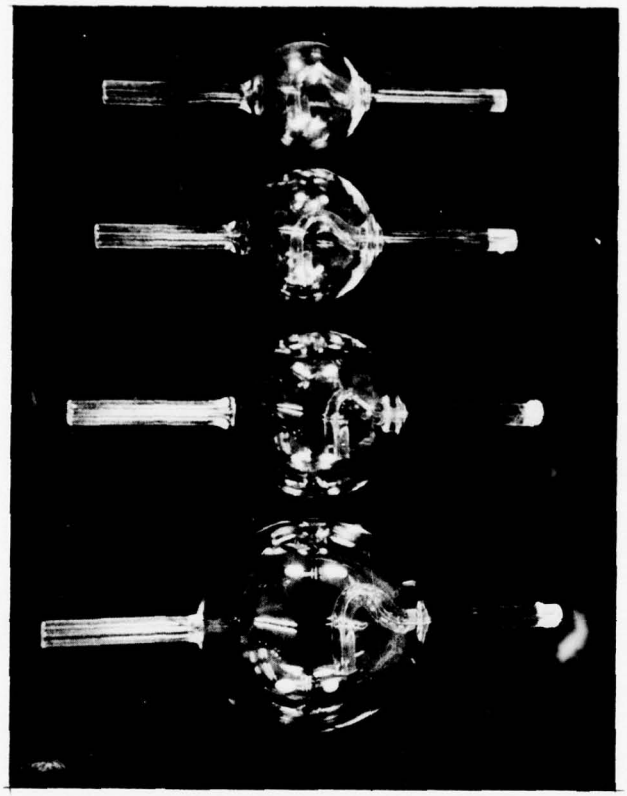


Figure 4 Reservoir Mixing Vessels for Growth of Epitaxial Layers with Graded Doping Profiles. The measured volumes are listed on the right.

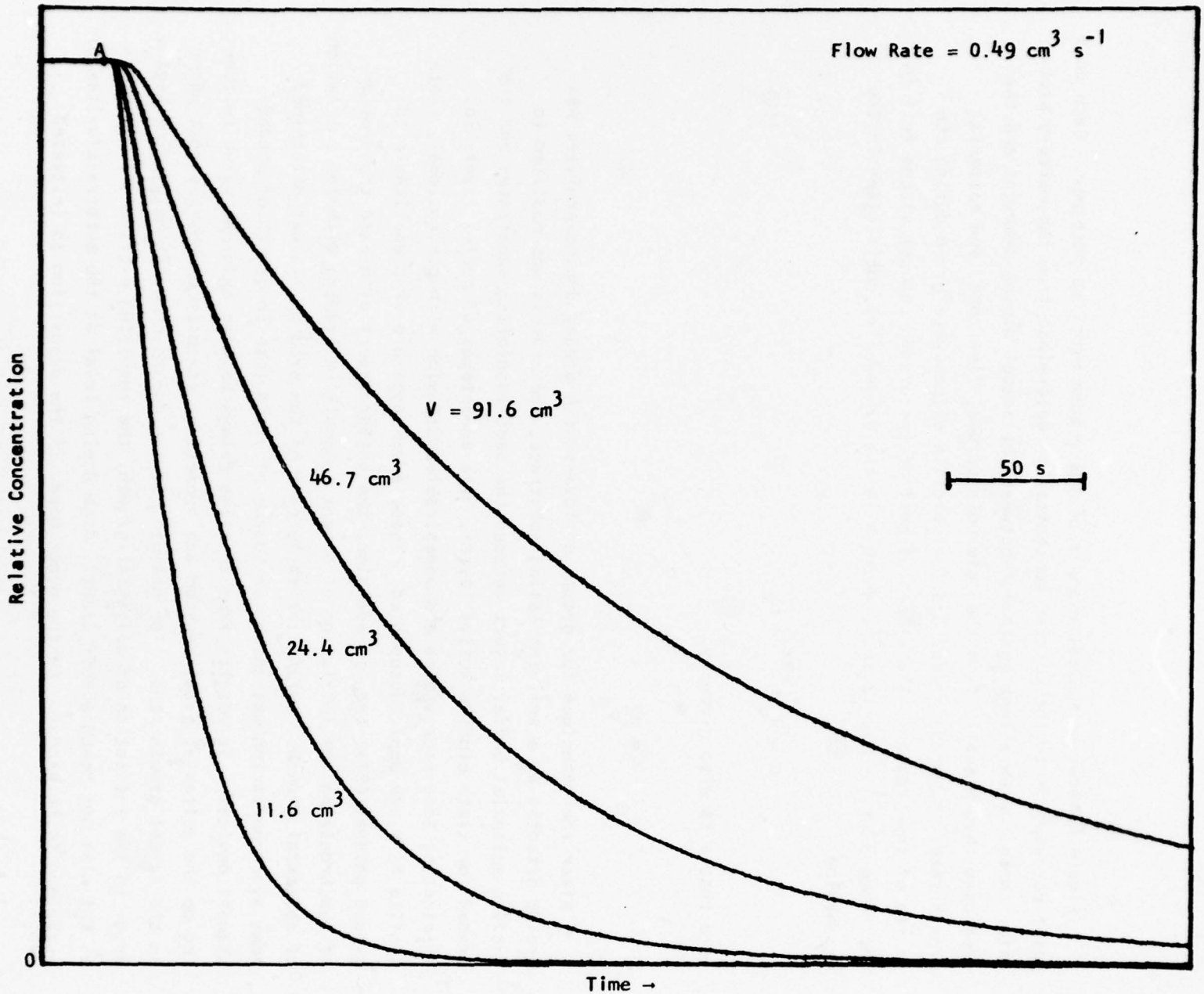


Figure 5 Gas Compositions as a Function of Time for Reservoir Vessels of Different Volumes (V)

Figure 6 shows a typical example of the graded profiles obtained. Each data point corresponds to the carrier concentration determined from the mercury probe data. Note the excellent agreement between the actual doping gradient and that predicted theoretically from the reservoir volume, flow rate, and epitaxial growth rate. Numerous graded and flat profile slices were grown during the course of the program. The slopes of most of the graded channel slices fell in the range $3\ \mu m^{-1} \leq \alpha \leq 12\ \mu m^{-1}$, where α is the exponential coefficient in the expression

$$n = n_o e^{-\alpha x} + n_\infty \quad . \tag{16}$$

Note that α is also given by

$$\alpha = \frac{vg}{V} \quad .$$

After the technique for growth of layers with graded doping profiles was proved directly on a semi-insulating substrate, the process was modified to include epitaxial buffer layers between the semi-insulating substrates and the graded (or flat) profile active layers. The advantages of buffer layers in eliminating interface states and undesirable diffusion with conventional, flat-profile FETs are amply documented. These advantages are also applicable to graded channel FETs; and, in addition, the buffer layers eliminate the problem of synchronizing the initiation of dopant composition grading with the initiation of epitaxial growth. During the early part of the program, it was determined that synchronization was the major source of yield loss in growth of graded channel devices. It results from the time delays between external valve switching on the epitaxial growth system and subsequent composition changes that occur in the actual growth zone. For example, if the dopant composition grading begins prior to the initiation of epitaxial growth, the resulting profile will be graded but will not reach a sufficiently high doping level at the substrate/epitaxial interface to be useful. On the other hand, if the deposition is initiated

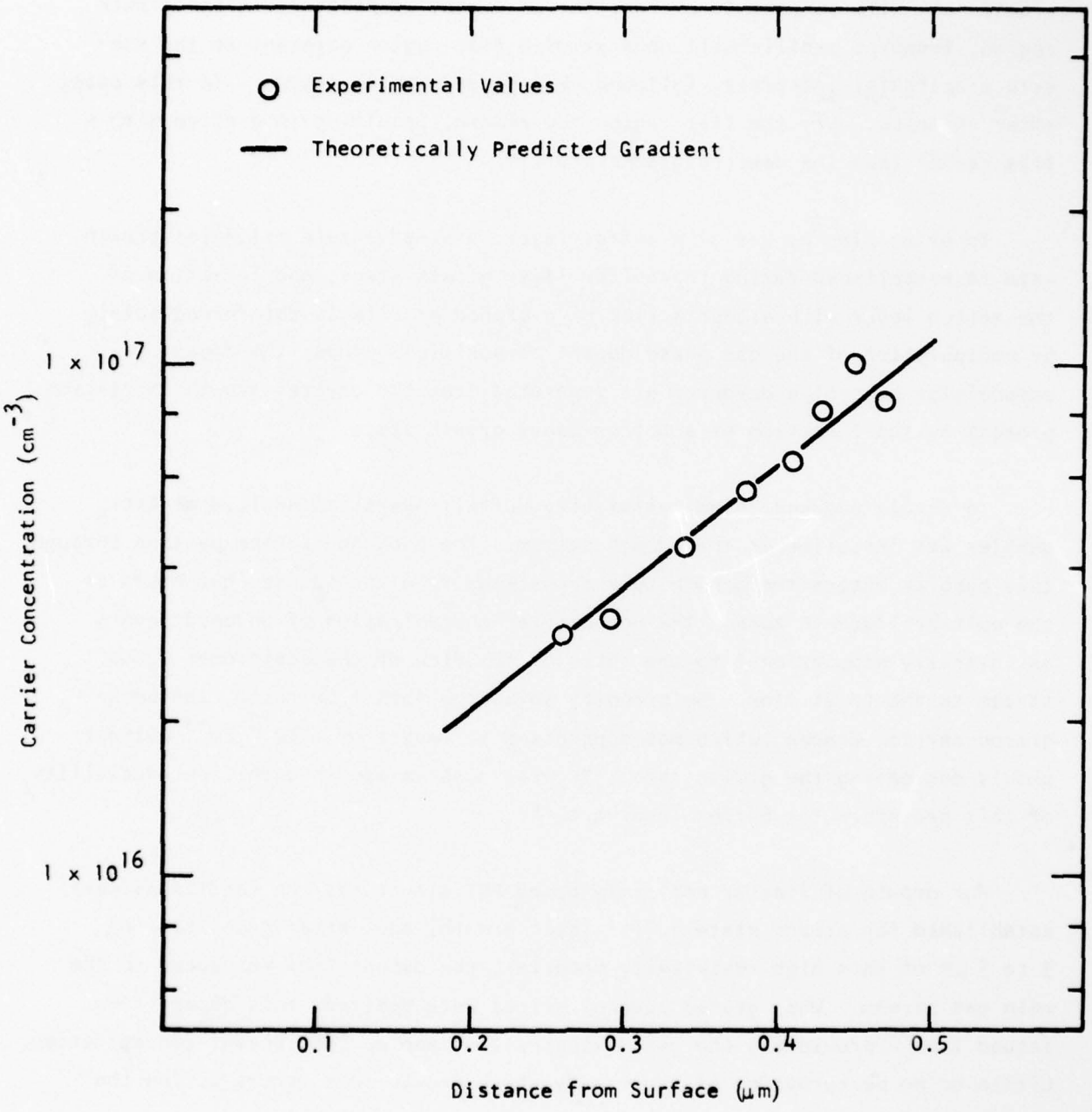


Figure 6 Doping Profile Determined from Hg Probe C-V Measurements. Line represents predicted gradient (dopant flow - 40 cm^3 min^{-1}, reservoir volume - 91.6 cm^3, growth rate - 0.083 μm min^{-1}).

prematurely with respect to the decline in dopant composition in the growth region, then the profile will consist of a flat region adjacent to the substrate/epitaxial interface, followed by a graded region beyond. In this case, after thinning, only the flat region may remain, resulting in a slice with a flat rather than the desired graded profile.

In principle, by use of a buffer layer, a steady-state epitaxial growth rate is established during the buffer layer growth stage, and formation of the active layer with either a flat or a graded profile is determined solely by manipulation of the gas phase dopant composition. Thus, the dopant composition control procedures are separated from the crystal growth initiation process by the insertion of a buffer layer growth stage.

To obtain undoped, high resistivity buffer layers, an additional $AsCl_3$ bubbler was installed in the growth system. The hydrogen stream passing through this bubbler enters the growth tube downstream from the source, but ahead of the epitaxial growth zone. The net carrier concentration of undoped layers is inversely proportional to the ratio of the flow of the additional $H_2/AsCl_3$ stream to the total flow. By properly adjusting this flow ratio, the background carrier concentration was suppressed to levels of $\sim 10^{13}$ cm^{-3} without unduly decreasing the growth rate. Several runs established the reproducibility of this procedure for buffer layer growth.

For growth of flat or uniformly doped FET structures the conditions were established for steady state buffer layer growth; and, after deposition of 3 to 5 μm of this high resistivity material, the dopant flow was added to the main gas stream. When graded channel slices were desired, this dopant flow issued from a previously charged mixing cell of appropriate dopant concentration. Little or no perturbation of the steady state growth rate occurs during the transition from buffer to active layer growth.

An example of the doping profiles obtained with this approach is shown in Figure 7. The buffer layer concentration is in the 10^{13} cm^{-3} range, and the active, graded layer has an intentional doping gradient of 1.7 decades per micrometer ($\alpha \simeq 4\ \mu m^{-1}$). Note the relative sharpness of the transition region between the buffer and active layers in the important doping region above 10^{16} cm^{-3}.

It was anticipated that formation of good ohmic source/drain contacts might be more difficult with graded channel or other FET structures with low surface carrier densities. While, in practice, little difficulty was encountered in formation of ohmic contacts to graded channel structures, a number of epitaxial structures were grown with n^+ epitaxial contact layers for evaluation purposes. The n^+ contact layers were grown sequentially after the graded, active layers during the same epitaxial deposition run. This approach avoids the potential problems of interfacial contamination and/or damage associated with the surface preparation inherent in a two-step process where the slice is removed from the growth apparatus prior to growth of the n^+ contact layer.

An example of the doping profiles produced in growth of the three-layer structures is given in Figure 8. A buffer layer, whose doping level is in the low 10^{13} cm^{-3} range, is first grown on the semi-insulating substrate. This is followed by the graded channel active layer with a peak doping level of 1.1×10^{17} and a controlled gradient of 2.4 decades/μm ($\alpha = 5.5$). The details of the graded active region are shown on an expanded abscissa scale in the inset. Later, the channel region was selectively thinned by the self-limiting anodization process (to be discussed later) to a depth of 1.8 μm below the original surface. The n^+ contact layer is formed last during the sequential deposition run and is doped in the high 10^{17} cm^{-3} region. Note the abrupt transitions between adjacent layers, a feature that is particularly important in growth of graded channel structures.

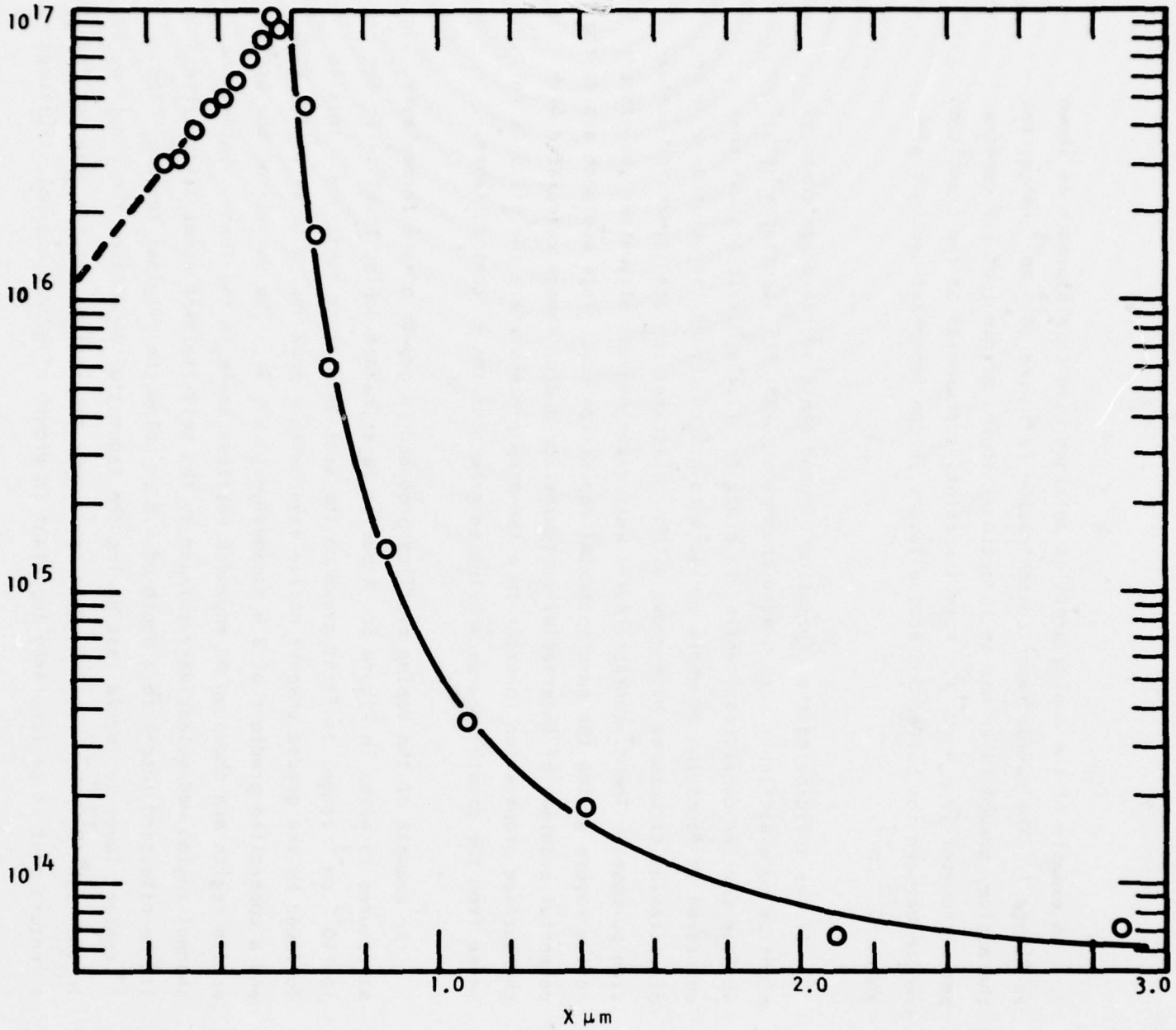


Figure 7 Doping Profile of Graded Channel Slice Incorporating an Undoped Buffer Layer

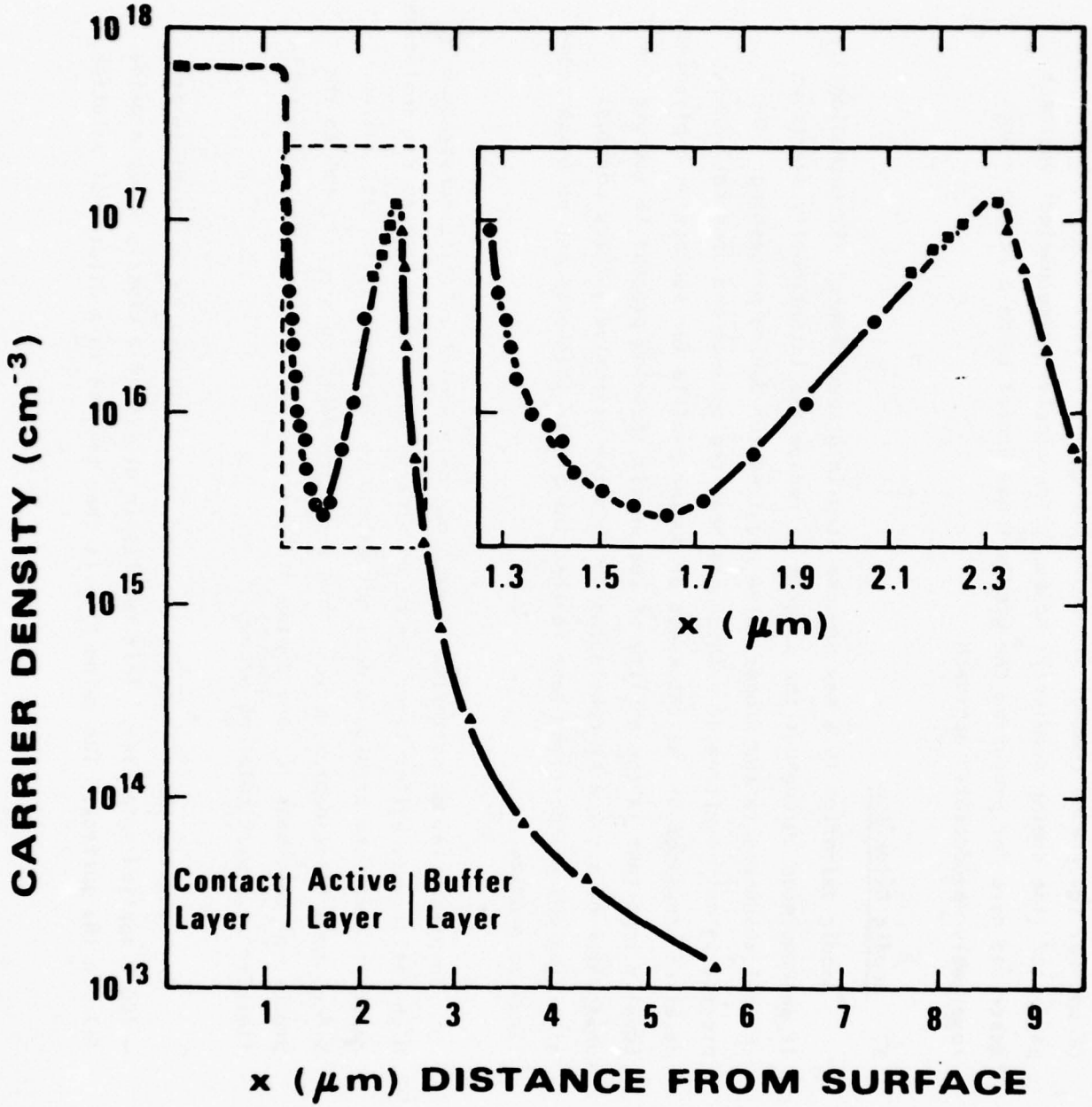


Figure 8 Doping Profile of a Graded Channel Slice Incorporating an Undoped Buffer Layer, a Graded Active Layer, and an n^+ Contact Layer

In general, after epitaxial growth of many companion flat and graded profile FET structures, it can be concluded that there is little difference in the run-to-run reproducibility and yield between the two basic structures. Of course, the graded channel structure introduces an additional control parameter (the doping gradient); however, the simple, nonmechanical approach described here for producing the gradient has proved to be a reliable and remarkably "producible" approach.

B. Anodic Oxidation

Anodic oxidation is a key process step in graded channel FET technology. It was employed throughout the program to reduce the intentionally overgrown channel thickness to the proper value required for device processing. The process is self-limiting at a thickness near the optimum and does not require detailed knowledge of the thickness or doping profile for successful application. Equally important is the ability of the anodic thinning process to improve the uniformity of a slice by continuing to thin the excessively thick portions after the thinner portions have reached the proper thickness and no longer continue to anodize.

In principle, an epitaxial layer grown on a semi-insulating substrate or high resistivity buffer layer can be anodically oxidized as long as the depletion depth at avalanche breakdown does not extend to the high resistivity region. Since, to a first approximation, this depletion depth is proportional to the product of thickness (ℓ) and doping density (n), the process tends to be self-limiting at a particular $n\ell$ product.

In practice, the slices are anodized in a 0.02M NaH_2PO_4 electrolyte at $\sim$ 100 V applied potential. This results in growth of a clearly visible oxide film on the surface. The oxide film is then removed in a dilute HCl solution,

and after careful rinsing to remove any traces of Cl^-, the process is repeated. Whenever any portion of the slice is thinned to the point that its local $n\ell$ product is less than the critical value, oxidation ceases, and that portion remains at a constant thickness while the remaining portions of the slice continue to be thinned. The process is continued until no visible oxide can be grown across the slice.

With graded channel slices, for a given peak doping density there is a maximum doping gradient that will allow anodic oxidation. Gradients in excess of this value will not provide a sufficient $n\ell$ product. When the gradient was too steep, the slices failed to grow a visible oxide, and the excessive gradient was easily diagnosed. This effect is illustrated by the plot given in Figure 9, where the peak doping densities of several slices are plotted as a function of their respective exponential grading coefficient (α) [cf. Equation (16)]. Solid circles in the figure indicate slices whose entire surface produced a visible oxide at the initial anodization step after growth. Partially and completely open circles designate slices that exhibit partial and no visible oxides, respectively. It is apparent that for visible anodic oxide formation to occur, the product of the peak doping density (N_p) and the exponential gradient coefficient (α) must correspond to

$$N_p(cm^{-3}) > 2 \times 10^{12}\ \alpha(cm^{-1}).$$

Development of a special procedure was necessary for slices with epitaxially grown n^+ contact layers to selectively reduce the layer thickness in the channel region to the proper value while leaving the n^+ contact regions intact. The initial approach, which is outlined in Figure 10, required first patterning the slice with a protective mask so as to selectively expose the channel regions. Photoresist was tried as a masking material, but it tended to become excessively undercut during the subsequent anodization process. Plasma-deposited Si_3N_4, however, proved quite stable and was adopted as the masking material.

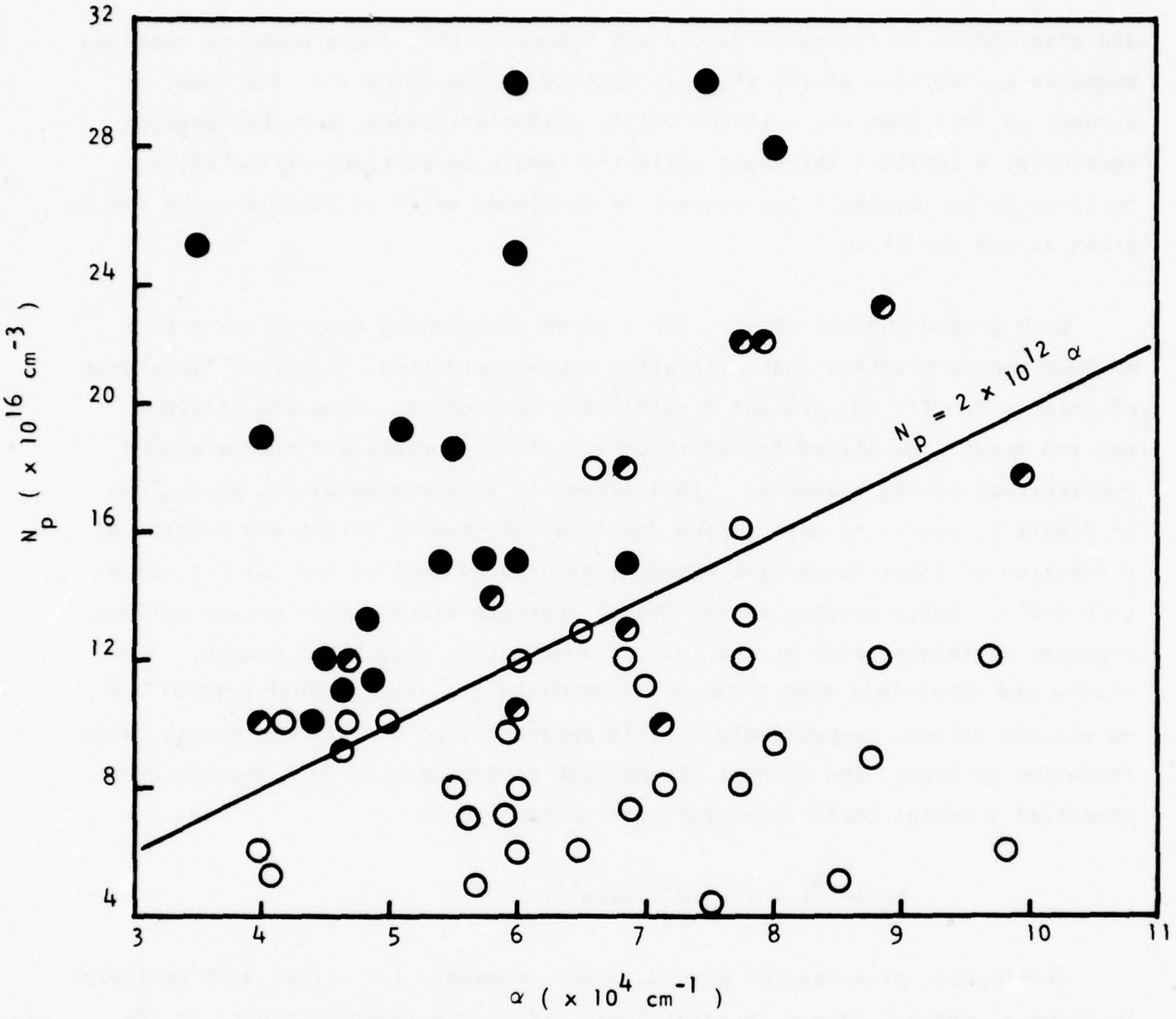


Figure 9 Effect of Exponential Doping Gradient (α) and Peak Doping Density (N_p) on the Appearance of Visible Oxides After Anodic Oxidation. Extent of slice surface coverage by visible oxide - ● complete, ◐ partial, ○ no coverage

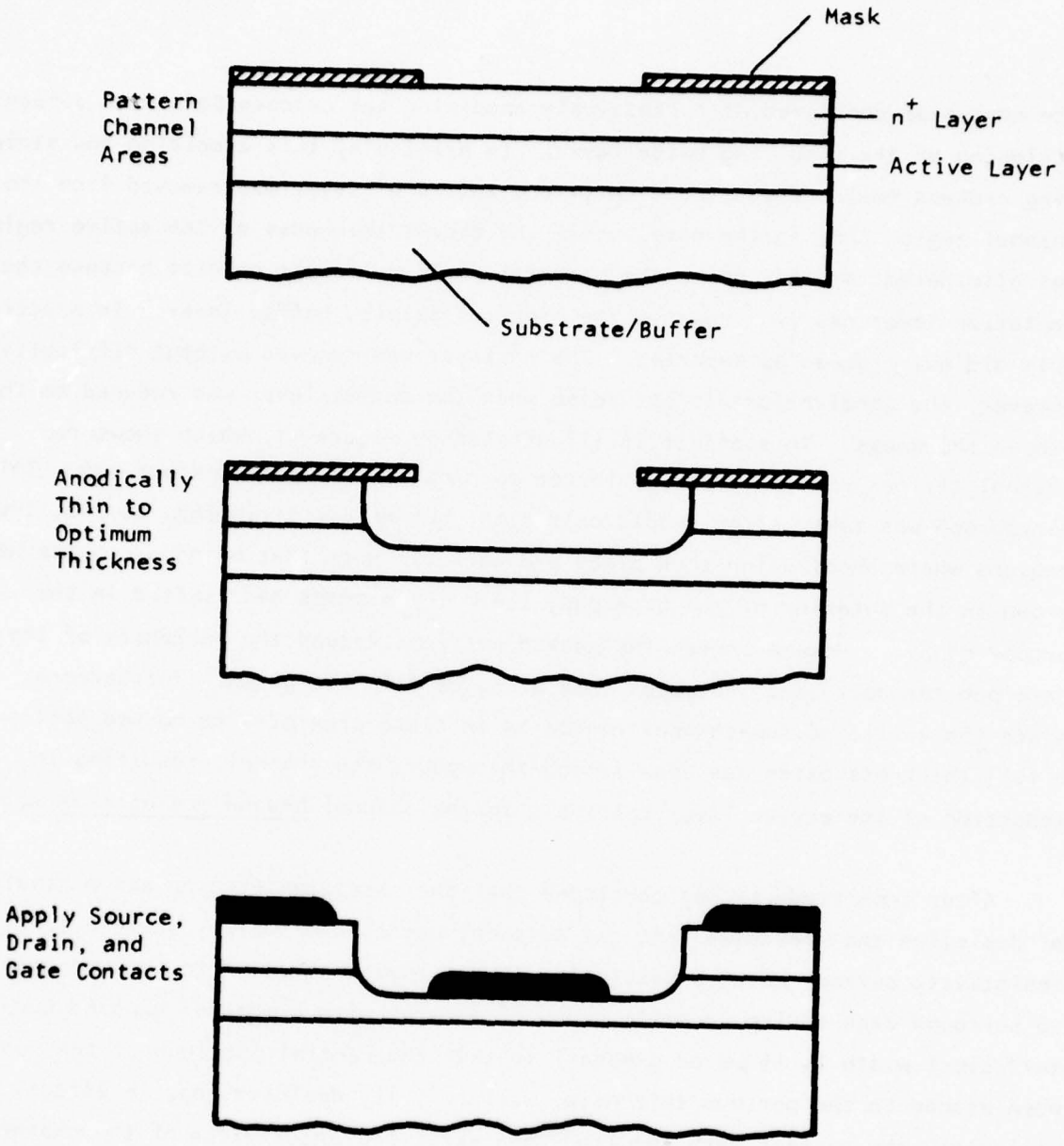


Figure 10 Localized Anodic Thinning

The next step consisted of successively anodizing the exposed GaAs with subsequent stripping of the resulting oxide layer. In principle, this anodizing and stripping process would be continued until the entire n^+ layer was removed from the channel region and, furthermore, until the excess thickness of the active region was eliminated; at that point the material would no longer anodize because the depletion layer has just reached the high resistivity buffer layer. In practice, this did not proceed as expected. The n^+ layer was removed without difficulty; however, the anodization did not cease when the active layer was reduced to the proper thickness. This effect is illustrated by Figure 11, which shows two channel stripes connected to the larger opening for the gate contact pad. This micrograph was taken after anodic oxidation, but before stripping, so that the regions where anodization took place are darker. Note that no anodic oxide was grown in the interior of the gate pad, i.e., the process had limited in the proper manner. However, near the masked portions around the periphery of the gate pad the dark band indicates that an oxide film has grown. Furthermore, since the entire narrow-channel region is in close proximity to masked portions, a full thickness oxide has been formed throughout the channel, resulting in reduction of the active layer thickness in the channel beyond the optimum value.

After some study, it was concluded that the excessive etching was a result of depletion and breakdown into the adjacent unetched material, where a low resistivity current path is available. The proposed solution to this problem was to surround each device or small group of devices with a moat of exposed GaAs of sufficient width ($\sim$ 15 μm or greater) so that the central portions of the moats, when etched to the optimum thickness, will be fully depleted and, in effect, will block the current path required when excessive anodization of the channel regions of the enclosed device(s) is attempted. Thus, by use of a grid of connected moats, each local region of device patterns would cease to anodize when the adjacent moats reach the proper thicknesses.

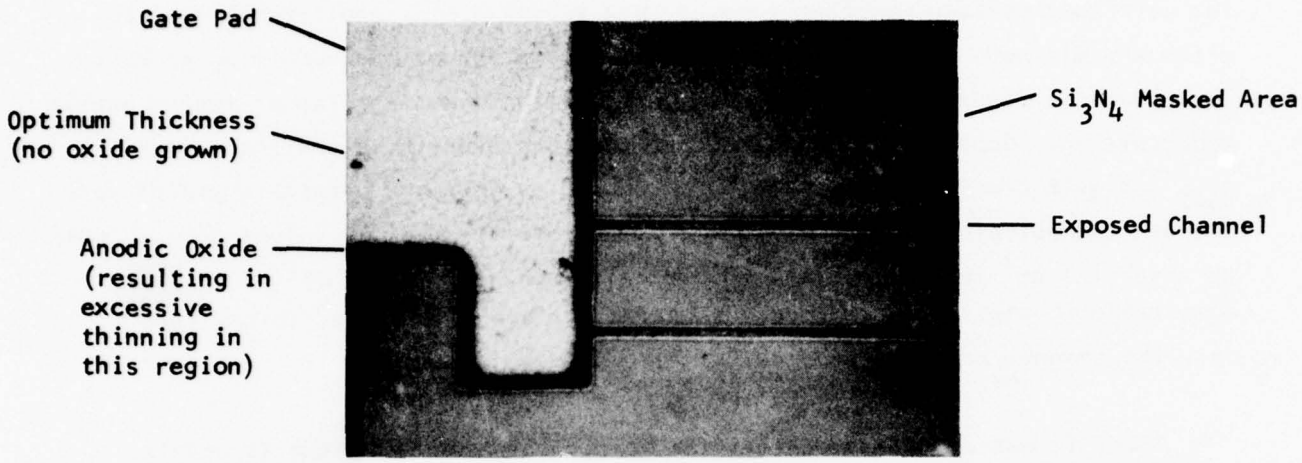


Figure 11 Micrograph of Selectively Anodized Gate Pattern

For evaluation of this approach, a special mask was made to define the required moat pattern. The gate and moat patterns were then defined in nitride and photoresist, and the slice was anodically thinned in the conventional manner. The gate/moat pattern was then removed, and source-drain metallization was applied and alloyed. Figure 12 shows an SEM photograph of the resulting geometry. The thinned channel is longer than the original gate pattern finger length due to undercutting. Subsequent measurement of the source-drain saturation current, I_{SAT} (no gate present) across the slice indicates that the procedure yields very uniform channel properties. For example, a measurement of 58 values of I_{SAT} over an area of 1 cm^2 resulted in a standard deviation of 3.3%. This value is comparable to that obtained when the entire surface of a slice, rather than only the channel area, is anodically thinned.

Thus, it was demonstrated that the anodic thinning technique is usable in the presence of n^+ material if the necessary moat pattern is present, that it remains self-limiting, and that it produces values of I_{SAT} that are uniform across the slice and have a value suitable for device fabrication. While this technique should be valuable for any slice having an n^+ epitaxial layer, it is particularly useful for graded slices, since they may involve the additional variation with respect to the doping gradient across the slice.

C. Device Design

Since the channel doping profile was the principle element being varied in these studies, all other aspects of the geometry and design of our contempory FET devices were retained. This facilitated the study of doping profile effects by eliminating the need to simultaneously consider the effect of other modifications. Three existing device geometries were used during the course of the program. Their features are summarized in Table 2. Each of the three device types is referred to by the total gate width of one cell.

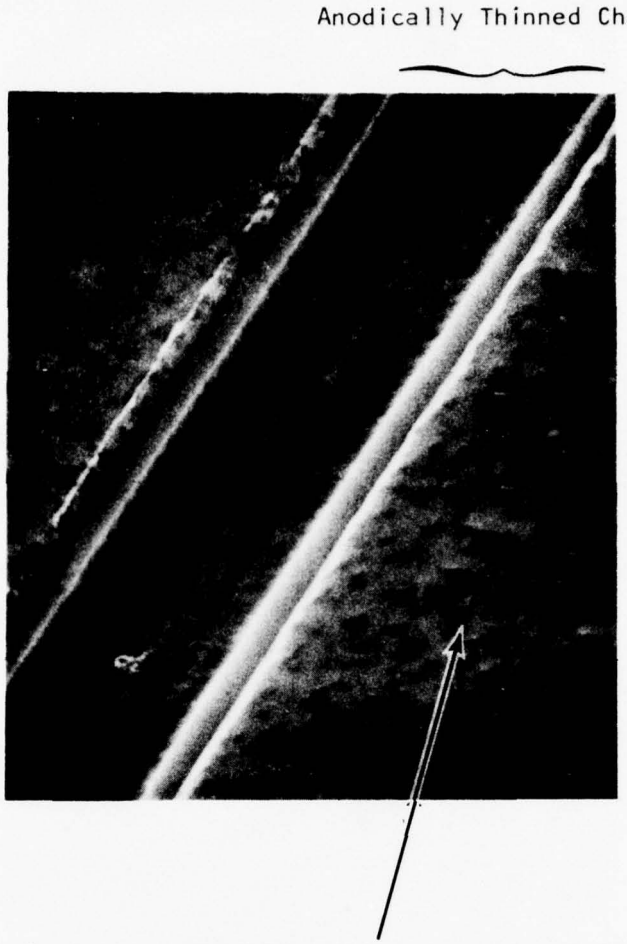


Figure 12 SEM Photogrpah Showing n^+ Ohmic Contacts and the Thinned Channel Produced by Localized Anodic Oxidation.

Table 2

Characteristics of the Three Device Geometries Used in the Program

Device Type (Gate Width Per Cell, μm)	No. Cells	No. Fingers Per Cell	Finger Length (μm)	Gate	
				Nominal Length (μm)	Method of Definition
600	4	4	150	2	Optical
1200	4	8	150	1*	E-beam
300	1	4	75	0.5 to 0.8	E-beam

* In some cases the gate length was different in each cell (see text)

The designation "600 μm devices" refers to four-cell devices, each cell having a 2 x 600 μm optically defined gate distributed over four fingers. The 300 μm devices are single-cell structures designed for small-signal, low-noise performance. They have electron beam defined gate fingers that are 75 μm wide and usually 0.5 μm to 0.8 μm long. The 1200 devices are four-cell devices designed for power applications. Each cell has a 1 x 1200 μm gate distributed over eight fingers. These gates are also defined by e-beam lithography. In some cases the e-beam machine was reprogrammed to produce a different gate length in each of the four cells. In this case the gate lengths usually ranged from 1 μm to 2.2 μm.

The remainder of this section gives a brief review of the various considerations involved in the design of the above devices.

- Gate Length

Gate length is the most important design factor in GaAs FETs for obtaining high gain and low noise at microwave frequencies. This is true for both uniformly doped and graded material. The effect of gate length on noise figure is indicated by the following equation[5]:

$$NF_{min} = 1 + KfL \left(\frac{n}{a}\right)^{5/6} \left[\frac{3.3\, w^2 p}{hL} + \frac{1.8\, L_{SG}}{na_1} + \left(\frac{0.18\, r_c}{na_2}\right)^{1/2}\right]^{1/2}, \quad (17)$$

where L = gate length (μm),
L_{SG} = source-to-gate separation (μm),
w = gate finger width (mm),
n = epitaxial carrier concentration (10^{16} cm^{-3}),

a = channel thickness beneath gate (μm),

a_1 = effective epitaxial thickness between source and drain (μm),

a_2 = channel thickness beneath source (μm),

h = gate metallization thickness (μm),

ρ = gate metallization resistivity (10^{-6} Ω-cm),

r_c = specific contact resistance (10^{-6} Ω-cm^2),

K = noise coefficient (0.033 to 0.036 for "good" epitaxial films).

In Equation (17) the three terms in the brackets are the contributions of, respectively, the gate metallization resistance, the parasitic source-gate resistance, and the ohmic contact resistance.

Equation (17) is used in Figure 13 to plot minimum noise figure as a function of frequency for several different gate lengths. The accuracy of this equation decreases at short gate lengths, since it does not include gate fringing capacitance and carrier velocity overshoot. Also, the minimum noise figure contains terms proportional to the frequency squared,[6] which reduces the accuracy of Equation (17) at high frequencies. In spite of these reservations, the equation may be used to determine the functional dependence of the minimum noise figure on any of its parameters, including gate length.

Device gain is proportional to g_m/C_g, where g_m is the transconductance and C_g is the gate capacitance. In the limit of large gate lengths where the gate may be treated as a parallel plate capacitor, the gate capacitance is proportional to gate length. At a given frequency, device gain increases and noise figure decreases as gate capacitance (and thus gate length) decreases.[6] The proportionality of gate capacitance to gate length is fairly accurate at gate lengths as small as 1 μm. However, gate fringing capacitance and various parasitic resistances are of increasing importance as gate length is reduced below 1 μm. For a gate length of 0.5 μm the fringing capacitance is more than 30% of the total gate capacitance[7]: this fraction would be even larger for still smaller gate lengths.

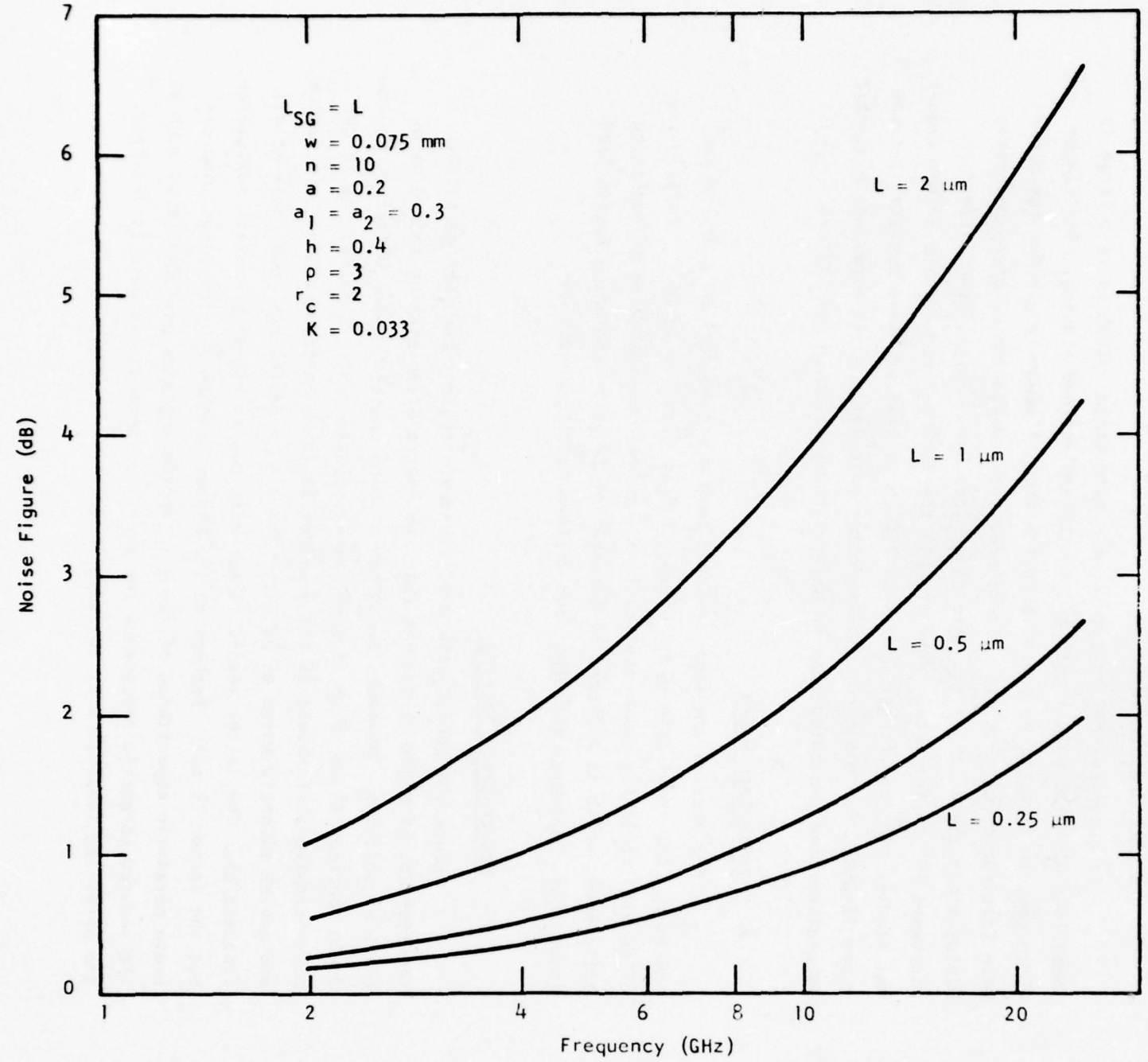


Figure 13 Calculated Dependence of Noise Figure on Frequency for Several Gate Lengths (individual devices) and the amplifier noise figure requirements.

- Gate Finger Width

In a typical FET structure, the gate finger width is very large in comparison with the gate length and the interelectrode spacing. The finger width can, in fact, be an appreciable fraction of a wavelength for the microwave frequencies of interest. Therefore, the propagation of electromagnetic fields along the width of the gate finger can have a significant effect on microwave FET performance. However, all the devices used for the graded channel studies had gate finger widths of 150 μm or less and were operated between 8 and 12 GHz. For these conditions, other calculations and experiments at this laboratory have indicated that no serious degradation in gain occurs.

- Total Gate Width

For most of the work reported here a single cell of a device was operated. The total gate width of the cell is given in Table 1. Paralleling of several cells for power applications involves consideration of combining efficiency, which is affected by a number of factors, including source lead inductance, impedance matching, and uniform feeding conditions.

- Source-Drain Spacing

Since the source-gate and gate-drain regions are just parasitic resistances, it might be thought that the source-drain spacing should be as small as possible. However, experiments using devices having different source-drain spacings (4 μm, 5 μm, 7.5 μm) have indicated this is false. At 10 GHz the microwave performance of the 4 μm device is no better than the 5 μm device and may be slightly worse at 12 GHz. The 7.5 μm device has lower gain at all frequencies. The latter result is expected due to higher parasitic resistance, but the former is not. Perhaps at the higher frequencies the larger source-drain parasitic capacitance of the 4 μm device degrades performance as much as the reduced parasitic resistance improves it. Because the gate is recessed, the parasitic resistance is not very large.

- Cell Size

It might be thought that as yield improved, GaAs FET cell size should be increased to reduce bonding complexity. However, in our experience cell sizes larger than ~ 1200 μm gate width should not be employed at X-band. With larger cells the source-lead inductance per unit gate width becomes excessive, and the cell impedance becomes difficult to match.

D. Basic FET Fabrication Process

No modifications in the basic fabrication process were necessary to process graded material. That basic fabrication process is described in this section. The modifications needed to process material having n^+ contact layers are described in the next section.

- Mesa Etch

The first step following receipt of the anodically thinned slices is to etch mesas through the active layer to isolate the source and drain except for the channel under the gate and to provide an insulating surface for the gate bonding pad. Proton bombardment ($10^{14}/cm^2$, 50 keV) has also been used to isolate devices, but this process has not been employed routinely.

- Source-Drain Metallization

The next step is source-drain metallization. The pattern is defined in photoresist, and the metal is evaporated over the slice and removed from regions where it is unwanted by dissolving the resist in acetone (the lift-off process). The metallization is about 2100 Å eutectic composition AuGe followed by 500 Å Ni. The contacts are made ohmic by alloying for one minute at 450°C in flowing He. This metallization system provides very smooth, low resistance contacts with sharp edge definition. The contact resistance is typically 0.3 Ω per mm gate width for slices having $n \sim 1 \times 10^{17}/cm^3$. The source-drain

spacing is much more reproducible with lift-off than with etching. No other ohmic contact system to GaAs reported in the literature gives such low contact resistances.

Since the doping concentration near the surface is lower in a typical graded device than it is in a typical uniformly doped device, it might be anticipated that the contact resistance of graded devices would be inferior to that of uniformly doped devices. In practice, this was only a minor effect. Test areas were used to routinely measure contact resistance on every slice processed for a period of one year. Although the average contact resistance of the uniformly doped structures was less than the average of the graded structures, the overlap of the two sets of measurements was substantial.

- Gate Definition

The next step is the gate metallization, which is also defined by a lift-off process. For the 600 μm geometry, which has a 2 μm gate, the gate pattern is defined optically in the same manner as the source-drain. For the other geometries gate definition is accomplished by electron beam. The electron resist is polymethyl methacrylate (PMMA), and the gate is lifted off with acetone similar to the source-drain metallization. The gates are automatically aligned within the source-drain gap using alignment marks in every 2 mm x 2 mm "field." These marks are "L"-shaped patterns and were put down with the source-drain metallization. The gate length can be varied by simply reprogramming the electron beam computer, and gate lengths of 0.5 μm or less are well within the machine's capability. The yield of devices with no shorted or open gate fingers following gate definition is substantially higher when electron beam definition rather than conventional contact printing is used, due to mask-slice abrasion and mask run-out with the latter. The PMMA thickness is 5000 to 7000 Å, and a 5000 Å metal film is readily lifted off.

An important step is to etch the slice slightly immediately prior to gate metallization in order to recess the gate below the epitaxial surface. This reduces the source-gate and drain-gate parasitic resistance and also modifies the electric field configuration below the gate. It has been found to improve device microwave performance significantly. Recessing the gate does decrease the device parameter uniformity slightly in some cases, but the performance improvement is so great that it is necessary. Aluminum has been employed as the gate metal because of the ease with which it can be evaporated and its ability to produce good Schottky barriers to GaAs, even after annealing at 400°C or more.

- Bonding Pad Metallization

Following gate metallization, a 0.5 μm layer of Cr/Au (defined by lift-off) is evaporated onto the source and drain to improve current spreading to the contact edges and bondability. A nitride layer is then plasma-deposited on the active areas to protect them from scratches and shorts to the source wires. Next, a 10 μm layer of Au is plated to the source and drain pads to aid in bonding, and the slice is lapped to 100 μm. The slice is then scribed or sawed into discrete devices.

E. Modifications for n^+ Contact Layers

Near the conclusion of the contract period, slices having an n^+ epitaxial contact layer were utilized to fabricate devices having n^+ material under the source and chain metallizations. This required several modifications in the normal fabrication process described above. Those modifications are described in this section.

The 600 μm geometry was used for all n^+ device fabrication. These devices have optically defined gates, and hence a gate mask was available for use in the localized anodic thinning process described in Section III.B. After mesas were

formed on the n^+ slice (which, of course, had not yet been anodically thinned), a 4000 Å thick layer of silicon nitride was plasma-deposited over the slice. Photoresist was applied next, and the gate pattern was aligned relative to the mesas and exposed. The moat pattern required for localized anodic thinning (see Section III.B) was available on another mask. This pattern was also aligned relative to the mesas and exposed in the same photoresist. Thus, after development, both the gate pattern and the moat pattern were defined in the resist. The slice was then plasma-etched to replicate these patterns in the underlying nitride. Two four-cell devices were within each isolated square of the moat pattern.

The slice was submitted for anodic thinning. This resulted in removal of all the n^+ material and a self-limited portion of the n layer in the exposed portion of the slice. Some undercutting occurred, so the thinned channel region was wider than the mask opening. After the nitride/resist mask is removed, fabrication proceeds in the usual manner. Figure 12 shows a SEM picture of the thinned channel region after the source-drain metallization has been applied and alloyed. For gate recess and metallization the gate pattern was reapplied and aligned to the thinned channel region. Processing then proceeded in the normal manner.

In one case, still another procedure was followed: the gate was applied before the source-drain. This simplified the processing because the gate pattern did not have to be applied twice. The gate pattern that was present for localized anodic thinning was also used for gate recess, metallization, and lift-off. The disadvantage of this procedure is that the source-drain current cannot be monitored during the critical gate recess step because no source-drain metallization is yet present.

The moat mask discussed previously had an active area smaller than the area of the slices used. As a result, the outer portions of the slice were anodically

thinned to completion. Hence, part of every n^+ slice processed had portions equivalent to the usual anodically thinned slices lacking an n^+ layer. This facilitated study of the effects of the n^+ contact layer, since companion devices having no n^+ material were simultaneously fabricated on the same slice.

SECTION IV
DEVICE EVALUATION

A. Dc Evaluation

The FETs examined initially were 600 μm optical gate geometry devices fabricated on material having no buffer layer. Flat profile and graded profile slices were grown in subsequent growth runs with the same reactor. These companion slices were then processed simultaneously. This procedure sought to minimize variations (other than doping profile) between flat and graded devices. Due to an insufficient gate recess, the first companion slices to complete fabrication yielded devices that did not pinch off. Nevertheless, these devices dramatically demonstrated the improved linearity that was anticipated for graded devices. Digital meters were used to measure the saturated drain current as a function of gate voltage. The results are shown in Figure 14. The improved linearity of the dc transfer characteristic of the graded devices is obvious.

To enable a quantitative measurement of the amount of curvature of the dc transfer characteristic, the data were used to make a least-squares fit to a quadratic:

$$I_{DS} = a_o + a_1 V_g + a_2 V_g^2 \quad , \tag{18}$$

where I_{DS} is the saturated source-drain current, V_g is the gate voltage, and the a_i are the various coefficients determined by the least-squares fit. Note that a_o corresponds to I_o, the drain current at zero bias; a_1 corresponds to the transconductance, g_m; and a_2 is the quadratic coefficient, which would be zero for an exactly linear transfer characteristic. In all cases, portions of the transfer characteristic within 10% of pinch-off were highly nonlinear and were not used in the quadratic fits. Results of this procedure for the devices described above are also presented in Figure 14. The quadratic coefficients of the graded devices are seen to be nearly an order of magnitude smaller than

Slice 17905-42 = Graded
Slice 17905-44 = Uniform

Least squares fit to $I_{DS} = a_0 + a_1 V_g + a_2 V_g^2$

Slice

42 ① $I_{DS} = 141 + 8.66\ V_g + .043\ V_g^2$, $r^2 = .999$

42 ② $I_{DS} = 157 + 6.57\ V_g + 0.000\ V_g^2$, $r^2 = 1.000$

44 ③ $I_{DS} = 127 + 13.7\ V_g + .355\ V_g^2$, $r^2 = 1.000$

44 ④ $I_{DS} = 124 + 14.8\ V_g + .395\ V_g^2$, $r^2 = 1.000$

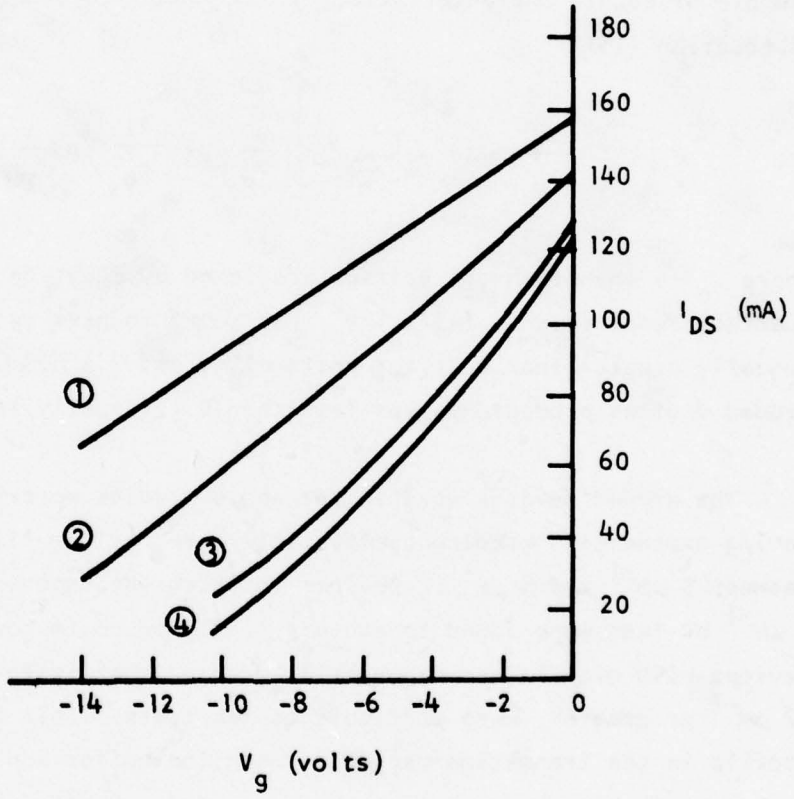


Figure 14 Dc Transfer Characteristics of Graded and Uniform Devices

those of the companion flats. The symbol r shown in the figure designates the correlation coefficient, which should be 1 for a perfect fit. As would be expected for gentle curves, the quadratic fits were always found to be excellent.

Subsequently, many companion flat and graded devices were fabricated. Material incorporating undoped buffer layers was used for these and all subsequent devices fabricated in the program. These graded devices also exhibited improved linearity of the dc transfer characteristic. Figure 15 shows a typical example of such a characteristic. It is useful to consider a "normalized" version of Equation (18):

$$\frac{I}{a_o} = 1 + \left[\frac{a_1}{a_o} V_p\right]\left[\frac{V}{V_p}\right] + \frac{a_2}{a_o} V_p^2 \left(\frac{V}{V_p}\right)^2 ,$$

where V_p is the pinch-off voltage predicted by Equation (18). The normalized quadratic coefficient, $(a_2/a_o)\ V_p^2$, was found to have values greater than 0.1 (usually greater than 0.2) for uniformly doped 2 x 600 μm devices, while the graded devices produced values less than 0.1 (usually less than 0.05).

The graded devices used in the above studies were fabricated from slices having exponential grading coefficients [see Section III.A, Equation (16)] between 5 μm^{-1} and 8 μm^{-1}. Devices in which the exponential coefficient was 3 μm^{-1} or less were found to exhibit little or no improvement in linearity. Devices with much larger exponential grading coefficients, on the order of 12 μm^{-1} or greater, were difficult to fabricate. This is because the doping profile in the transition region between the buffer and the graded, active layer is not perfectly sharp, but slightly rounded. Hence, in a steeply graded device having a sufficiently thinned channel to allow pinch-off, this transition occupies much of the active channel, and the doping profile is not a true exponential.

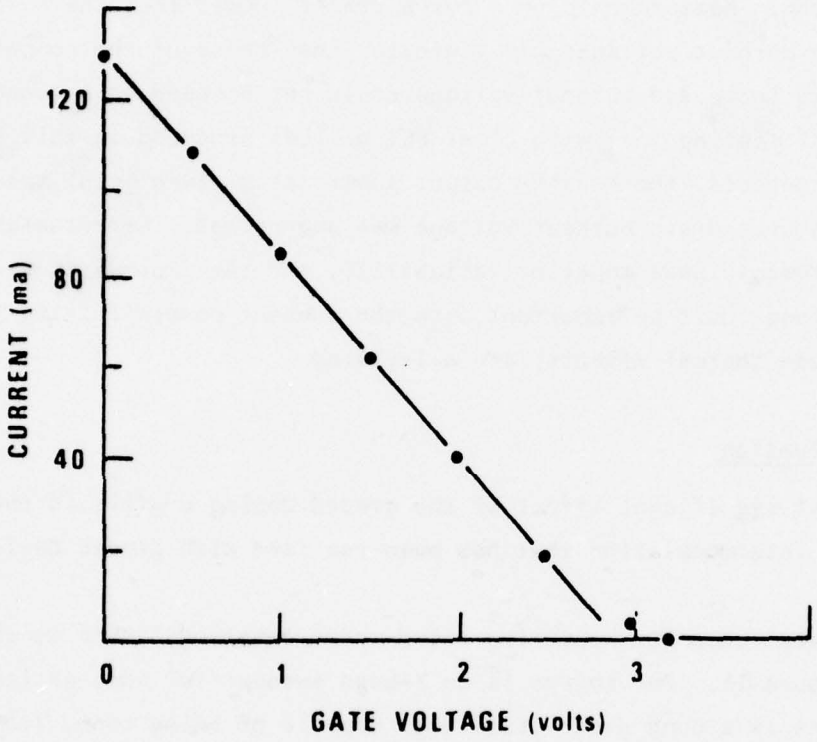


Figure 15 Dc Transfer Characteristic of a Graded Channel FET

- N^+ Devices

As described in Section III.D, devices having n^+ material under the source and drain metallization were fabricated near the program's conclusion, and each slice contained "control" portions that yielded normal FET structures for comparison. Measurements on a curve tracer showed that the n^+ devices had source-drain burnout voltages ~10 V greater than those of the comparison devices. However, this increased burnout voltage could not be used advantageously during subsequent rf testing. As with other FET devices produced in this laboratory without n^+ contacts, the maximum output power (at a given gain) saturated well before the source-drain burnout voltage was approached. Nevertheless, these n^+ devices presumably have superior reliability, and the improved source-drain burnout voltage could be important once the present power-limiting mechanisms (which include thermal effects) are alleviated.

B. Rf Evaluation

The most significant effect of the graded doping profile is the improved third-order intermodulation that has been realized with graded devices.

The system used for measuring third-order intermodulation is schematically shown in Figure 16. One source is an X-band sweeper/TWT combination, while the second source is a Gunn diode oscillator capable of being tuned from 8.7 to 12 GHz. In a few cases it was replaced by a second sweeper/TWT combination. The system is capable of supplying 17 dBm input power (per tone) at the device being tested. The output goes to both a power meter and a spectrum analyzer. Insertion of a test circuit fixture containing a short (instead of a device) showed that the system produced no measurable intermodulation of its own.

Third-order intermodulation (3IM) is a complex phenomenon that is influenced by many operating parameters, including drain voltage, gate bias voltage, and impedance matching. A device tuned for maximum gain at one input power level

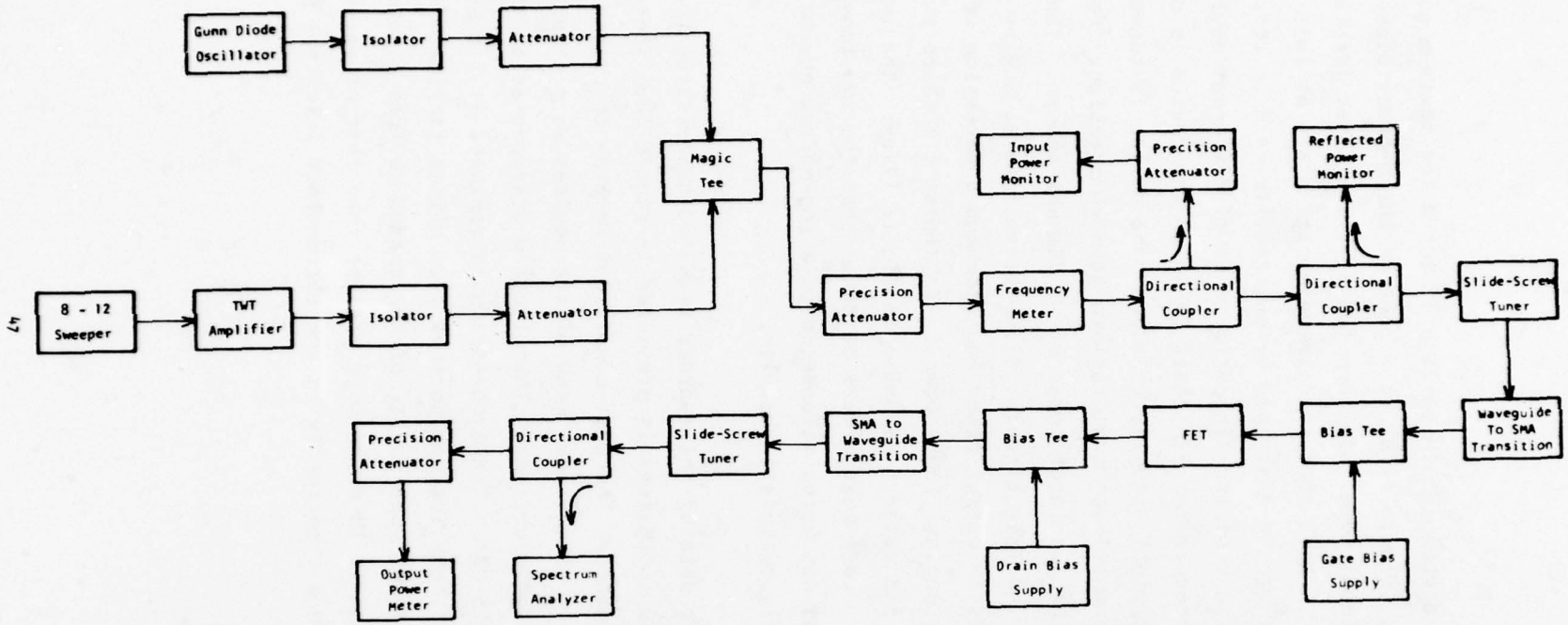


Figure 16 Block Diagram of Third-Order Intermodulation Microwave Test Set-Up

will usually show a changed 3IM pattern if tuned for maximum gain at another input power level. Figure 17(b) is a plot of third-order sideband suppression as a function of input power per tone for a device tuned for maximum gain at 13 dBm input power. Note that the plot exhibits a dip at this point. All these effects, and others to be described below, require care in attempting to make meaningful comparisons of the 3IM performance of different devices. Hence, we have adopted a procedure for 3IM tests in which the device is operated in a manner in which it might actually be used: the device is tuned for maximum gain at an input power level that is into gain compression. For our geometries and cell gate widths, an input power of 17 dBm was chosen. Tuning was accomplished by using chips on the test circuit, slide-screw tuners, and by adjusting gate bias. Measurements of output power and sideband suppression were then made as a function of (decreasing) input power. In almost all cases this resulted in a smooth, typical 3IM pattern as shown in Figure 17(a). The two tones were 5 to 10 MHz apart. Care must always be taken that the two tones and the third-order sidebands are not being attenuated by a too-narrow device bandwidth, which could lead to overly optimistic results.

Representative data of third-order sideband suppression for graded and uniformly doped 600 μm devices is presented in Figure 18. These devices had 2 μm optically defined gates. The test conditions were as described above. At the initial 17 dBm input power level many of the devices were clipping, as evidenced by the presence of gate current. The clipping disappeared as the input power was reduced below 15 dBm. These devices were operated at 9.5 GHz using 5 V source-drain bias. They include devices from slices fabricated over a six-month period. The consistent superiority of the graded devices is obvious. The sideband suppression is 10 dB or more greater than that of uniformly doped devices. This corresponds to a superiority in the third-order intercept point of 5 dB or more.

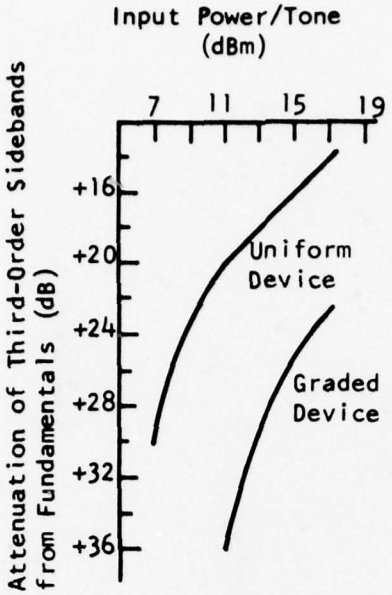


Figure 17(a) Third Harmonic Measurements for Devices Tuned to Maximum Gain at 17 dBm Input Power

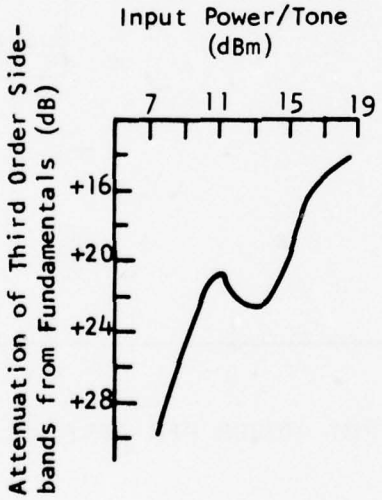


Figure 17(b) Typical Pattern of Devices Tuned for Low Sidebands at 13 dBm

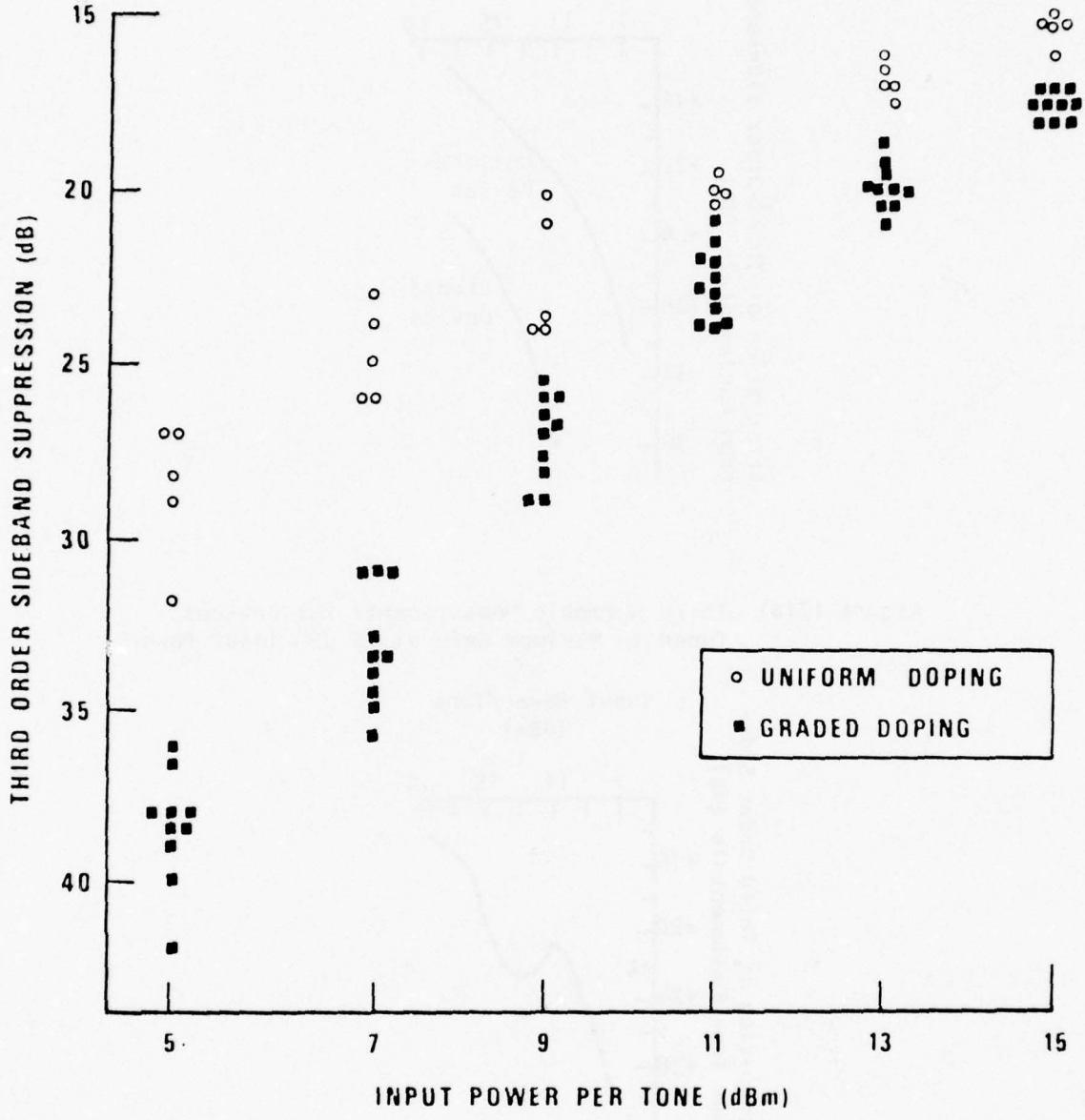


Figure 18 Comparison of Third-Order IM Performance of Graded Channel and Uniformly Doped FETs. All devices were tuned for maximum gain at 17 dBm input power and 9.5 GHz.

All these devices, both graded and uniformly doped, exhibited gains between 6.5 and 7.5 in the linear region. This was still under the condition of no retuning at these lower power levels. Thus, the actual small signal gain would have been higher if the device had been retuned for small signal operation. For these structures the 1 dB gain compression point for uniformly doped devices occurred near 12 dBm input power, and near 15 dBm for graded devices. This larger gain compression point for graded devices is due to the related decrease in the dc transconductance g_m and the increase in the pinchoff voltage V_p that result from the graded structure.

All the above results were obtained by operating only one cell of the device. Experiments in which two and four cells were used produced the expected results. For example, operating two cells produced twice the fundamental power, twice the third-order sideband power, and hence the same sideband suppression (measured in dB). Thus, to the extent that cells or gate width can be combined efficiently, total output power may be increased with no degradation in sideband suppression. This means, for example, that for a given device, doubling the total gate width will increase the third-order intercept point by 3 dB.

It should also be noted that if the above test condition of "no retuning" was violated, and the device was retuned at some lesser input power level, then it was almost always possible to obtain significant improvement in third-order sideband suppression (at that power level) with minor associated decreases in gain. Often, a 10 dB or more improvement in sideband suppression could be obtained at the cost of only a few tenths of a decibel in gain.

A striking effect that occurred for both graded and uniformly doped devices was a significant improvement in sideband suppression which occurred as the source-drain bias was increased. An example is given in Figure 19. Note that a change from 5 V to 8 V drain bias improved the sideband suppression by over

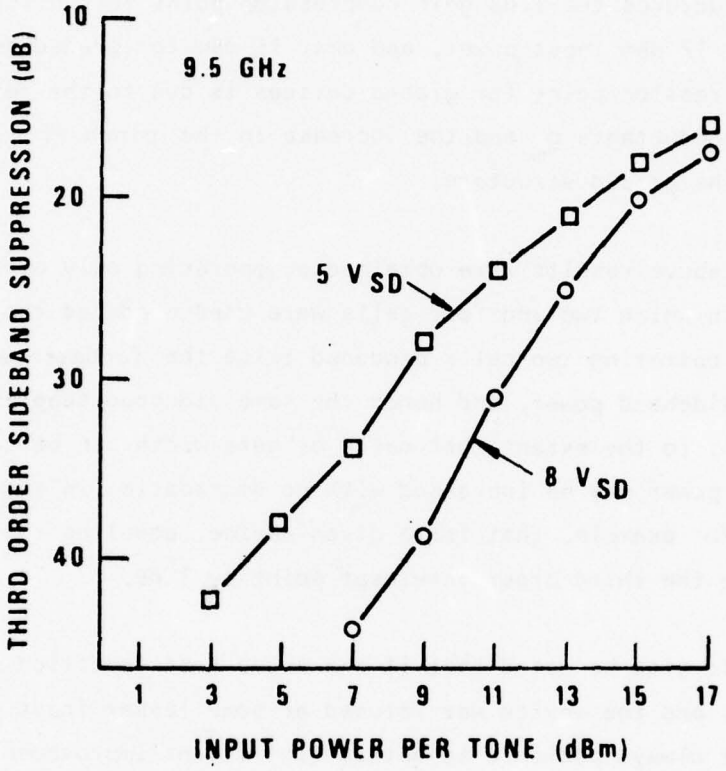


Figure 19 Third-Order Sideband Suppression as a Function of Input Power for Two Values of Source-Drain Voltage

10 dB, and hence the third-order intercept point by over 5 dB. At the same time, of course, the 1 dB gain compression point is increased. The devices were retuned for maximum gain at 17 dBm after a change in source-drain bias. Nevertheless, improvements in sideband suppression occurred even before this retuning.

Some investigation was also made of third-order intermodulation as a function of frequency by running tests at 8, 9.5, and 12 GHz. No systematic variation was observed between 8 and 9.5 GHz. However, at 12 GHz the sideband suppression was more than 5 dB greater than at 9.5 GHz. Gain was greatly reduced. Impedance effects are suspected to be the cause, as it was not possible to make the bond wires short enough at 12 GHz to resonate the device impedance (hence, the inordinately low gain).

All the above results were obtained using the 2 x 600 μm gate devices. Nevertheless, the detuning effects and increased drain bias effects, both of which improved sideband suppression, were also observed in subsequent work using the devices having 1 x 1200 μm and 0.5 x 300 μm gates.

Third-order intermodulation tests using the 1200 μm devices showed essentially the same results as those obtained earlier using the 600 μm devices, after the factor of two in total gate width was taken into account. Nevertheless, the intermodulation differences between uniformly doped and graded devices did not seem quite as large as those of the 600 μm devices. Extensive work with the 300 μm structures (0.5 to 0.8 μm gates) using devices from many slices led to the inescapable conclusion that the distinct and reproducible intermodulation improvements observed for the graded 2 x 600 μm devices simply were not apparent in the 300 μm structure. Nor was any improvement in the shape of the dc transfer characteristic observed.

Part of the reason may be that the 300 μm devices, being low noise structures, are usually fabricated with thinner channels (to produce lower pinch-off voltages) than devices with other geometries. Thus, a significant portion of the active channel may be occupied by the rounded transition region between the buffer and the clearly graded region. In fact, one slice of 300 μm graded devices that had an inordinately high pinch-off (6 V instead 2 to 3 V) did show some improvement in the shape of the dc transfer characteristic. However, the third-order intermodulation results were not superior.

These results with the 300 μm devices (0.5 to 0.8 μm gates) and the above results with the 1200 μm devices (1 μm gate) in which the observed improvement using graded devices appeared to be slightly less than when using the 600 μm devices (1.8 to 2 μm gates) led us to question whether gate length had any effect on intermodulation. Thus, in the later part of the program, several uniformly doped and graded slices were processed to produce 1200 μm devices in which each of the four cells had a different gate length. This was made possible by reprograming the electron beam machine that defines the gate pattern. The exact gate lengths varied from run to run, but could be measured using a scanning electron microscope. Figure 20 shows an example of such gates. Data from a uniformly doped device having gate lengths of 1.0, 1.4, 1.7, and 2.2 μm is shown in Figure 21. As expected, the shorter gate length cells exhibited higher gain and a higher saturation current. However, third-order intermodulation tests showed that the shorter gate cells exhibited the poorest sideband suppression [Figure 21(b)]. This pattern was true of graded devices as well. Although a few exceptions did occur, in which one cell having a longer gate length was slightly inferior to the next cell having a shorter gate, the overall pattern was clear. The shorter gate length devices had inferior intermodulation performance when run under the standard test conditions (tuned for maximum gain at 17 dBm input power).

Comparison of the results of such tests using devices from several uniformly doped and graded slices indicate that as the gate length is reduced, the difference

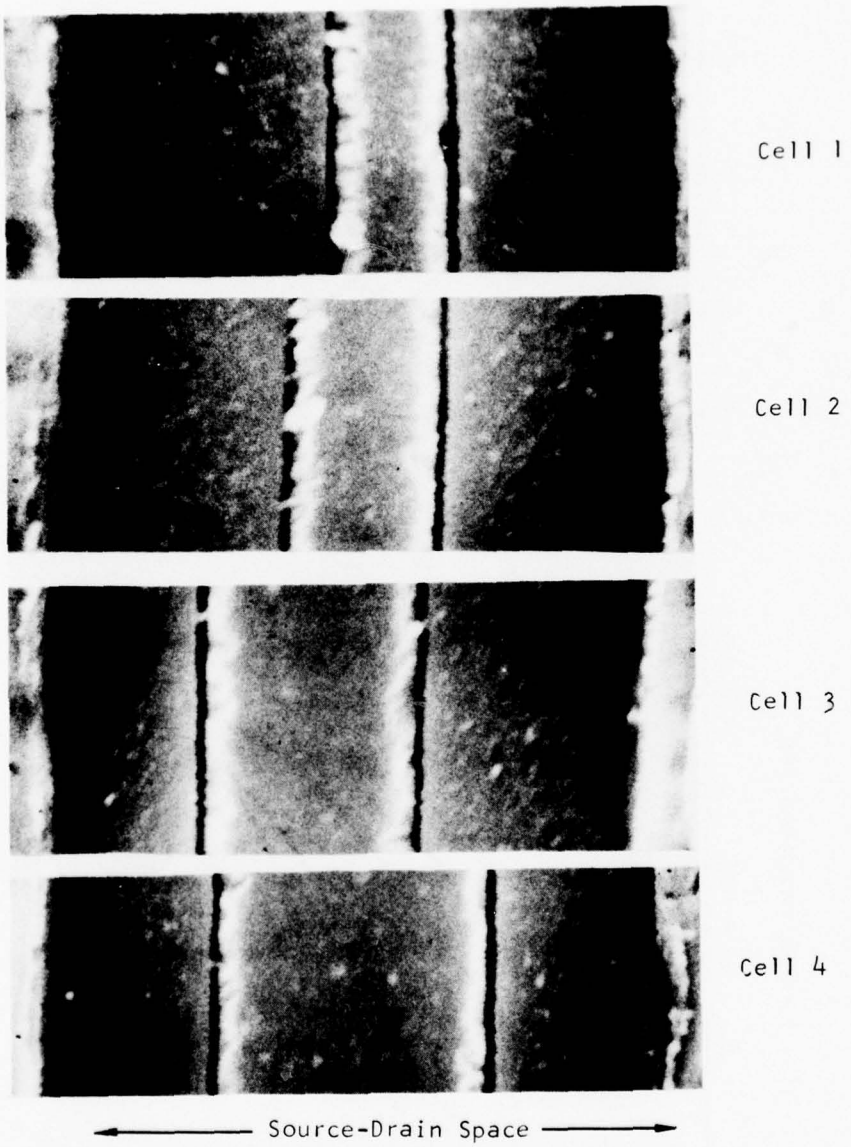
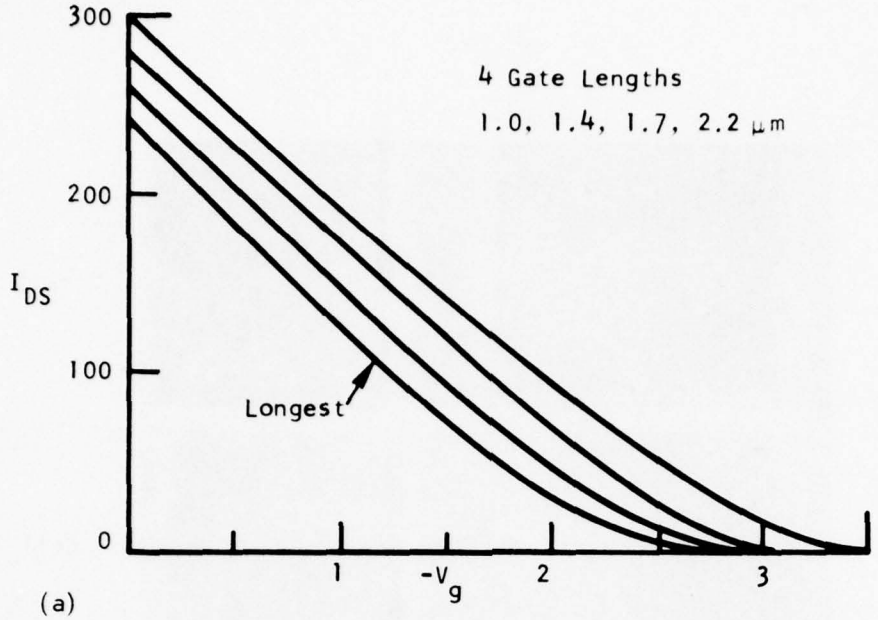


Figure 20 SEM Photographs Showing the Different Gate Length in each Cell of a 1200 μm Device



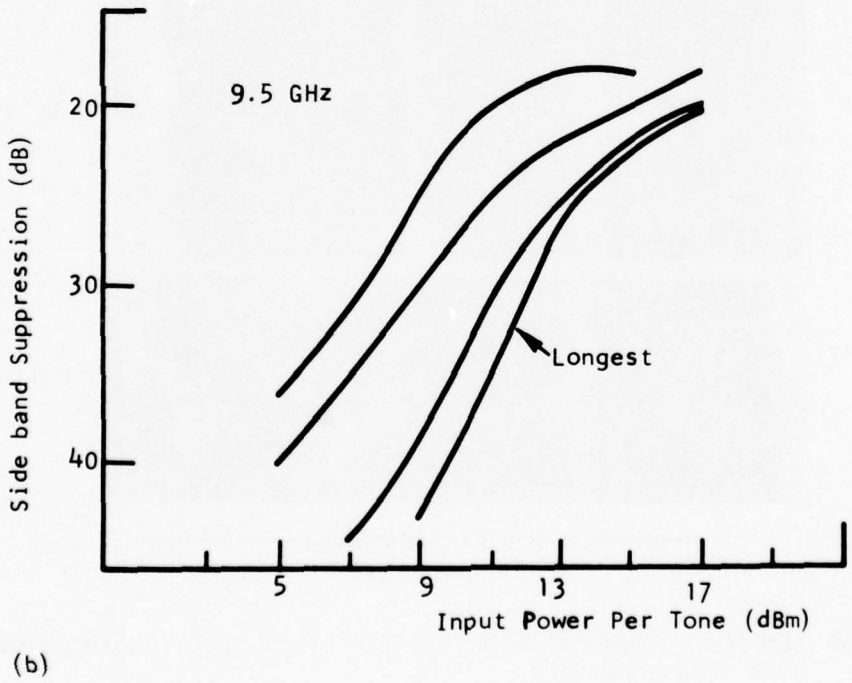


Figure 21 (a) Transfer Characteristics for Four Cells of a Single Device, Each Cell Having a Different Gate Length (1.0 to 2.2 μm). (b) Third-Order Intermodulation Data for the Same Four Cells

in intermodulation performance of normal and graded devices decreases. For gate lengths less than 1 μm the graded devices are superior by only a few dB. These conclusions should not be regarded as firm because of the limited number of slices that could be processed before the program concluded, and also because the four gate lengths varied slightly from slice to slice.

1. Noise Figure

As indicated in Section II of this report, the ability of graded devices to maintain a high value of transconductance near pinch-off implies that they should have a superior noise figure. Tests using the 600 μm devices (2 μm gates) showed this to be the case. Representative data are given in Table 3. Although results from only one uniformly doped slice are included in the table, those results are consistent with many other measurements made using devices of this geometry during the course of other studies. The minimum noise figures of the graded devices are approximately 1 dB lower than those of the normal devices. Obviously, this geometry is not a low noise structure and it was originally hoped that graded 300 μm devices (0.5 μm gates) would produce record noise figures. However, the failure of the 300 μm devices to show graded effects, reported above for intermodulation, also extended to noise figure performance. The noise figures of the graded 300 μm devices were not noticeably better than those of uniformly doped devices.

2. S-Parameters

A graded channel FET chip with known doping profile and a companion flat profile chip were characterized and compared in terms of their two-port S-parameters. The results are shown in Table 4. This table also includes the results of a flat TI power device from Reference 8. The measurements were made for small-signal conditions only using a Hewlett-Packard automatic network analyzer.

Table 3

Noise Figures at 9.5 GHz of Graded and Flat Profiled FETs

(Single-cell devices, 600 μm x 2 μm gate distributed over four fingers. All values in dB)

		At Maximum Gain		At Minimum Noise Figure	
		NF	G_{Max}	NF_{Min}	Associated Gain
Graded					
SLICE A	1	7.7	8.2	3.1	4.4
	2	7.0	6.7	2.9	3.9
SLICE B	1	5.2	6.8	3.4	3.9
	2	7.4	8.0	3.2	4.4
	3	4.6	7.2	3.4	5.0
Flat					
SLICE C	1	9.2	6.0	4.3	4.6
	2	9.8	7.6	4.3	5.2

Table 4

S-Parameters and Associated Maximum Available Gain (MAG) and Stability Factor (K) of 600 μm x 2 μm GaAs FETs as a Function of Frequency

	Frequency (GHz)	S_{11}	S_{21}	S_{12}	S_{22}	MAG	K	Bias Voltage
GC 77A1-143a #2-1 HP Automatic Network Analyzer	7.0 GHz	0.781 /-121°	1.429 /74°	0.088 /25°	0.673 /-31°	9.8dB	1.06	V_{GS} = -2.0 V
	7.25	0.769 /-122°	1.359 /73°	0.088 /25°	0.664 /-27°	9.1	1.19	V_{DS} = 6 V
	7.5	0.768 /-128°	1.268 /67°	0.084 /20°	0.642 /-32°	8.2	1.36	I_{DS} = 0.097 A
	7.75	0.78 /-130°	1.223 /65°	0.084 /18°	0.607 /-31°	7.8	1.44	
	8.0	0.763 /-134°	1.175 /61°	0.085 /18°	0.54 /-33°	6.7	1.69	
Flat 77A1-144 HP Automatic Network Analyzer	7.0	0.775 /-126°	1.59 /66°	0.048 /26°	0.763 /-37°	11.8	1.25	
	7.25	0.768 /-128°	1.508 /65°	0.049 /25°	0.749 /-33°	11.0	1.43	V_{GS} = -2 V
	7.5	0.771 /-134°	1.4 /59°	0.045 /23°	0.714 /-37°	9.9	1.75	V_{DS} = 6 V
	7.75	0.786 /-136°	1.35 /57°	0.046 /21°	0.668 /-36°	9.3	1.9	I_{DS} = 0.0828 A
	8.0	0.782 /-140°	1.321 /52°	0.047 /21°	0.583 /-40°	8.3	2.23	
TI Flat Power HP Manual Network Analyzer **	7.0	0.770 /-138°	1.18 /55°	0.075 /22°	0.61 /-78°	8.7	1.3	V_{GS} = -1 V
	7.5	0.75 /-145°	1.2 /49°	0.08 /24°	0.63 /-66°	8.4	1.31	V_{DS} = 7 V
	8.0	0.74 /-149°	1.16 /42°	0.074 /21°	0.66 /-75°	8.2	1.39	I_{DS} = 0.25 A

** See Reference 8

The FET chip was mounted as described earlier and placed in 50 ohm microstrip circuits in and out. The chip was then bonded to the 50 ohm transmission line with 25 μm (1 mil) diameter, 250 μm (10 mil) long gold bond wires. S-parameters thus measured included two bond wires as part of the device.

Figures 22 and 23 show the measured small-signal S-parameters of 600 x 2 μm graded channel and flat profile companion slice GaAs MESFET chips from frequencies 7 to 8 GHz. This device size was chosen because of its distinct graded profile property in combination with an input impedance level high enough to be measured accurately in a 50 ohm system. Previous experience showed that the real part of FET input impedance becomes smaller as device size increases to the point where it was increasingly difficult to measure with accuracy. The devices were biased to -2 V for gate and 6 V for drain to obtain high values of $|S_{21}/S_{12}|$ at 8 GHz. The magnitude of S_{21} was observed to increase rapidly as drain voltage increased from 0 to 4 V and reached a maximum above 5 V for both types of devices. Gate bias was held constant at -2 V. Above 5 V it was primarily the phase that changed with increase in drain voltage. The magnitude of S_{12} decreased as drain voltage was increased above 2 V.

The measured results indicate no significant differences between small-signal S-parameters of the graded channel and its flat profile companion slice for the input and output reflection coefficients S_{11} and S_{22}. The measured results did indicate, however, that the graded channel FET had a slightly lower forward transmission coefficient $|S_{21}|$ and approximately twice the reverse transmission coefficient $|S_{12}|$ of the companion slice.

In terms of the gain of the device, a larger $|S_{12}|$ indicates increased feedback and a corresponding reduction in isolation between the device's input and output port. This is evidenced by the maximum stable gain of the device according to the following expression:

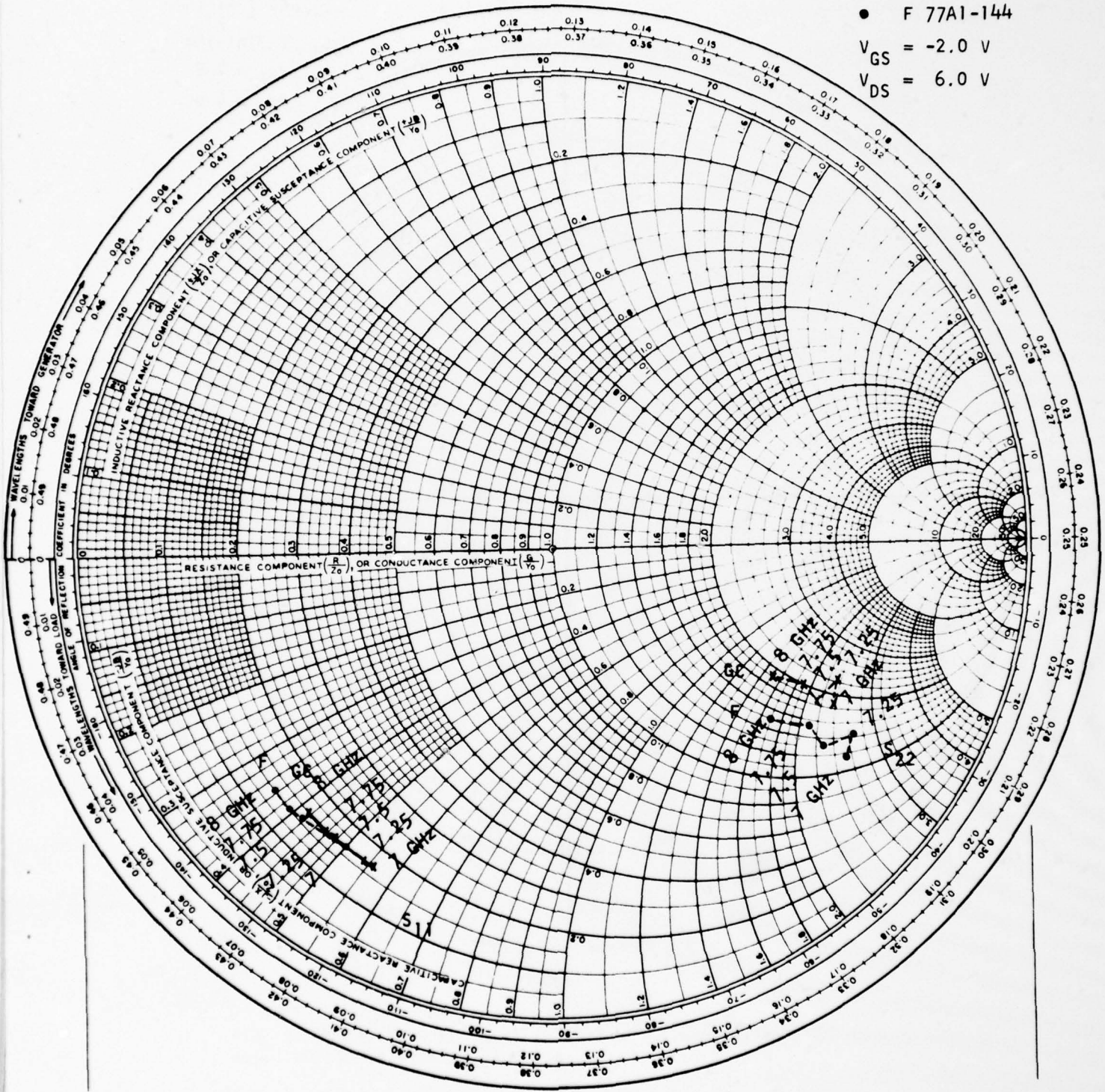


Figure 22 Small-Signal S-Parameters (S_{11} and S_{22}) of 600 μm Gate Width, Graded Channel and Flat Profile Companion Slice GaAs FET

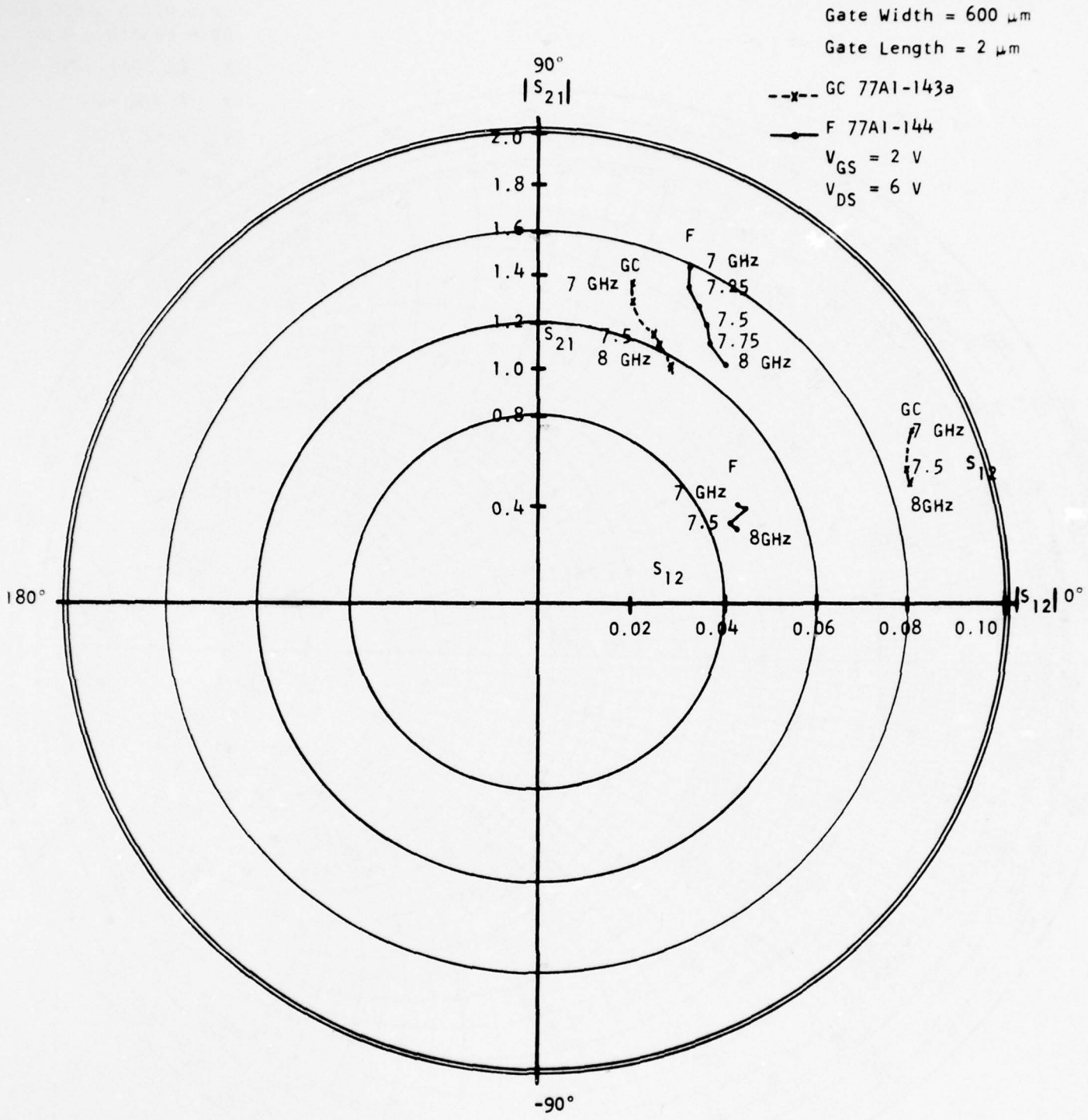


Figure 23 Small-Signal S-Parameters (S_{21} and S_{12}) of 600 μm Gate Width, Graded Channel and Flat Profile Companion Slice GaAs FET

$$\text{Maximum Stable Gain} \quad MSG = \left| \frac{S_{21}}{S_{12}} \right| \quad .$$

Plots of FET output reflection coefficient S_{22} versus frequency on the Smith chart (see Figure 22) consistently deviate from the constant conductance circle that is normally expected. This may be due partly to the mounting scheme employed to minimize circuit parasitics, which, in turn, may have caused these parasitics to resonate with the device output at these frequencies. Much larger gain roll-off characteristics than the usual 6 dB/octave observed for these devices may indicate either that some ground problems and gaps are associated with the test fixture used or that the bandwidth investigated was too narrow to observe the general gain roll-off trend.

3. Amplifier Characteristics

The expected improvement in linearity of the graded channel FETs over the uniform channel FETs was investigated by fabricating and testing microstrip amplifiers incorporating the optimized graded channel and flat profile FETs. Although it is adequate to compare device performances with given doping profiles and gradients in a narrowband, tuned amplifier, it is desirable to fabricate and test microstrip amplifiers using these devices to explore fully the power, gain, bandwidth potential, and linearity of these amplifiers, since the intermodulation distortion levels of power FETs are found to be sensitive to tuning.[9]

To obtain higher output power and efficiency, power amplifiers are driven with an ac input power of sufficient magnitude to operate the device beyond the linear region and where distortions will be generated in the amplifying device. With bias voltages held constant, this large ac input power changes the drain current and causes a shift in the dc operating point of the amplifier. For an amplifier with bandwidth of less than an octave second-order products should not

be too troublesome, since they are attenuated by the outband characteristics of the matching circuit. However, the third-order products are prominent and create signal distortions because they usually fall within the bandpass of the amplifier.

Preliminary distortion properties of FETs were assessed by three interrelated rf measurements at various input drive levels:

(1) Gain compression

(2) AM-to-PM conversion

(3) Third-order intermodulation.

In addition, gain and maximum output power as a function of frequency and amplifier sensitivity to bias voltage variations were measured. The results were compared to determine the relative merits of the two types of amplifiers for linearity performance.

Figure 24 shows a block diagram of the rf scheme for measuring gain compression, AM-to-PM conversion and bias sensitivities. A tunable Gunn oscillator capable of operating from 8.8 to 10.2 GHz provided frequency control of the test signal. The signal was amplified by the MESFET amplifier and monitored by power meter A. The input power level to the FET under test was set by precision attenuator A, while power meter B was calibrated to read the output power. The amplifier gain was determined from the readings of power meters A and B and precision attenuator A. The output was also coupled through a 10 dB coupler to the precision attenuator B, and then to the phase detector, completing the test channel leg of the phase bridge. The reference channel of the phase bridge was made up of a precision phase shifter, a level set attenuator, and a length of transmission line. The transmission line was used to equalize the time delay of the two channels. The precision phase shifter was used to null the phase bridge under various test conditions and hence to provide the relative phase data for phase response characterization. The output of the phase detector was

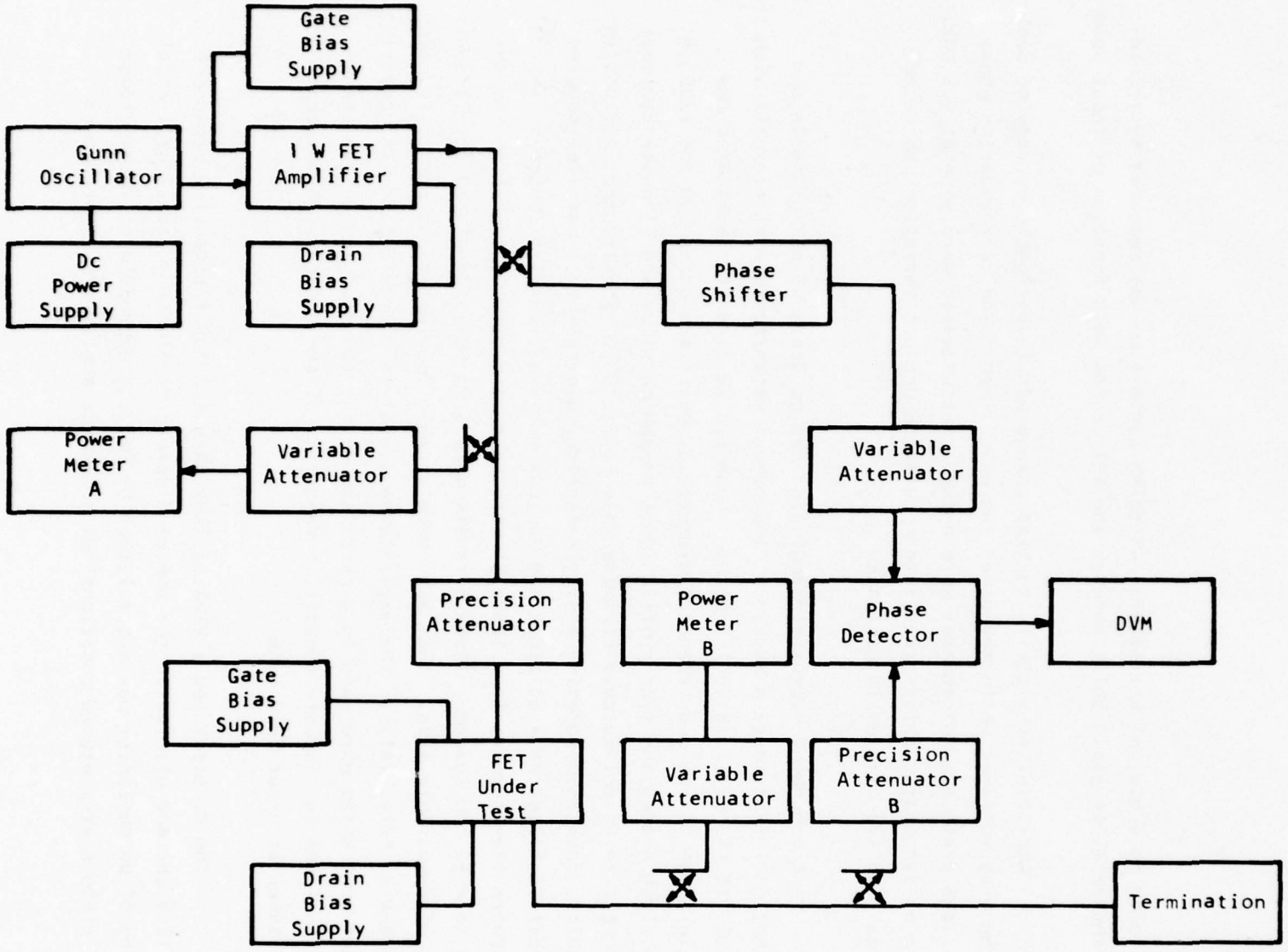


Figure 24 Rf Measuring System for Gain Compression, AM to PM Conversion, and Bias Sensitivities

monitored by a digital voltmeter. AM-to-PM conversion was measured by recording the relative phase shift through the FET device as a function of input power.

Amplifier sensitivity to bias change was investigated by varying one of the bias voltages while the other was held fixed. The corresponding phase, gain, and drain current changes were noted. Measurements were made at 9.5 GHz, since no systematic third-order intermodulation product variation was noted between the frequencies investigated.

A broadband microstrip amplifier can be designed using small- and large-signal S-parameters and input and output matching network elements with the CAINO2 (TI CAD optimization) program. However, we directly fabricated the single-stage narrow and broadband microstrip amplifiers using 600 and 1200 μm gate width graded and flat profile (both companion slice and TI power devices) GaAs FETs in a semi-matched circuits (see Figure 25). Input-output microstrip circuits, each incorporating a single-section, quarter-wave, parallel-coupled microstrip filter as a dc block and various multisection distributed series impedance transformers (see Table 5) were used to partially transform the device to a 50 ohm system. These circuits were orignially developed for TI power FETs of comparable size. They were used in this application to partially match FETs and quickly evaluate the amplifier's linearity and gain-bandwidth potential. Longer bond wires were used to connect the device to input and output transmission lines to resonate capacitive reactance of the device with the bond wire inductance at upper band edge.

The dc block had a VSWR of less than 1.2 for frequencies between 8 and 12.4 GHz and eliminated the use of discrete dc blocking capacitor. Final tuning of an amplifier was accomplished by welding appropriately dimensioned gold ribbons at pretuned positions for broadband amplifiers. Narrowband

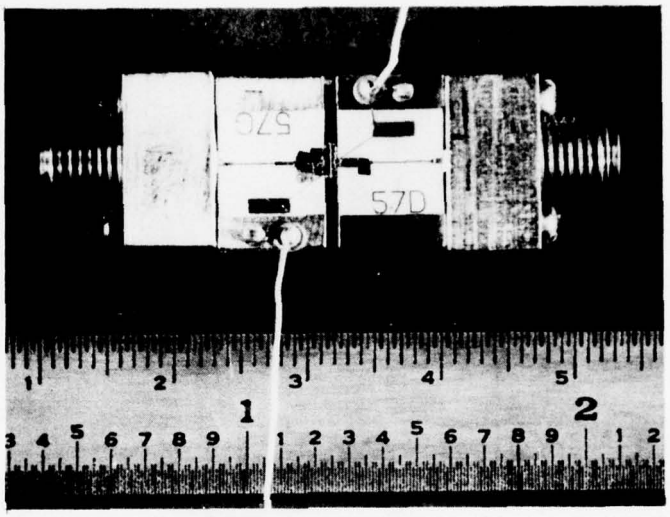
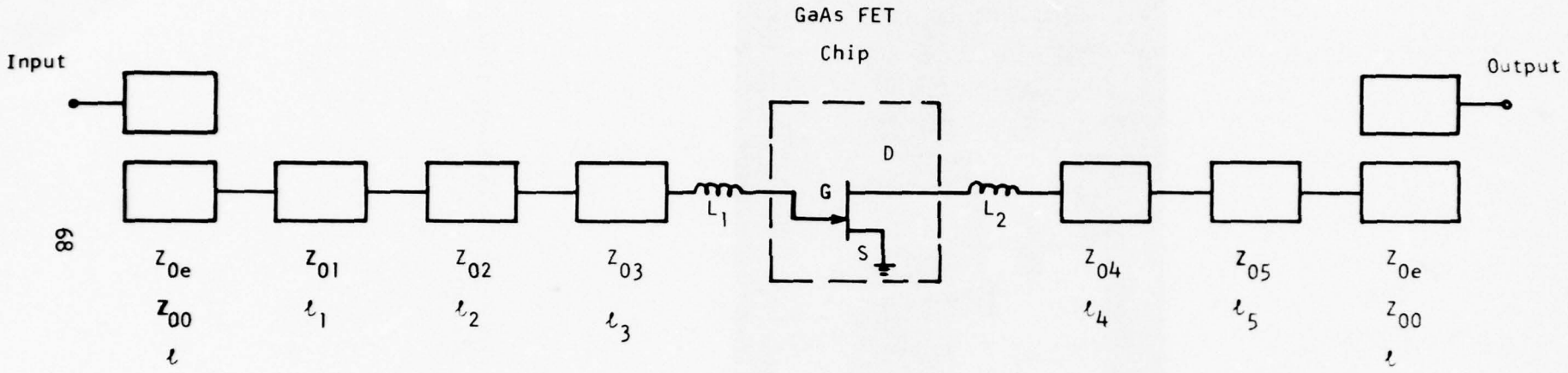


Figure 25 Photograph of a Single-Stage, Broadband, 1200 μm Gate Width, Graded Channel GaAs FET Amplifier

Table 5

Semi-Matching Circuits for 600 and 1200 μm Gate Width GaAs FET Amplifiers



Reference Frequency = 10 GHz

Circuit No.	Device Size (μm)	Input Circuit						Output Circuit				Interdigitated dc Block		
		$Z_{01}(\Omega)$	$\ell(\lambda)$	$Z_{02}(\Omega)$	$\ell_2(\lambda)$	$Z_{03}(\Omega)$	$\ell_3(\lambda)$	$Z_{04}(\Omega)$	$\ell_4(\lambda)$	$Z_{05}(\Omega)$	$\ell_5(\lambda)$	$Z_{0e}(\Omega)$	$Z_{00}(\Omega)$	$\ell(\lambda)$
56GD	600	38	0.086	34	0.0998	52	0.06	33	0.156	55	0.126	137	40	0.27
57GD	1200	50	0.134	33	0.119	16	0.097	29	0.189	50	0.057	137	40	0.27

amplifiers were chip-tuned. All amplifiers were biased with constant bias source to obtain large-signal maximum gain at the indicated frequencies.

The results of the amplifier evaluation (see Table 6) can be summarized as follows:

- The 1 dB gain compression point occurred at 16 dBm input power for the 600 μm graded channel amplifier and at 13 dBm input power for the flat companion slice at 9.5 GHz (see Figure 26). This difference may be due partly to a variation in the impedance matching achieved; i.e., small-signal gain was also different for these amplifiers, as discussed earlier, and may explain some of the differences observed in the AM-to-PM conversion of the two types of devices. However, even accounting for the above, the graded channel amplifier has less AM-to-PM conversion. A gain expansion of 1 dB maximum was observed for a 1200 μm, graded channel, narrowband amplifier (see Figure 27). Therefore, 1 dB gain compression for this amplifier was found to be an ill-suited specification for determining deviations from linearity. The gain expansion may be due to tuning near the power level where gain is being traded for better intermodulation distortion[9] and the variation of the device's output capacitance with drain voltage may have caused detuning and gain expansion effects. For 1200 μm broadband amplifiers, the 1 dB gain compression point occurred at 21.9 dBm input power for the graded channel device and at 21 dBm for the flat companion slice amplifier at 8.6 GHz and 9.5 GHz, respectively (see Figure 28).

- AM-to-PM conversion for 600 μm amplifiers measured at 9.6 GHz remained below 1.2°/dB maximum for graded channel as compared to 3.7°/dB maximum for flat profile amplifiers up to power levels of 15 dBm (Figure 29).

- Amplifier sensitivities to bias voltage variation of graded channel and companion slice FET amplifiers at 9.5 GHz indicated that insertion phase was extremely sensitive to the gate bias variation (18°/V) but not to the drain bias variation (4.5°/V) (see Figure 30). The gain was insensitive to the gate voltage

Table 6

Summary of AM-to-PM and Gain Compression Characteristics of 600 μm and 1200 μm Gate Width GaAs FETs

Device No.	77A1-143a #3-4	77A1-143a #4-1	77A1-144 #1-3	77A1-144 #2-3	77A3-73Ib #1-4	107AIIb-HA	77A1-145IIIb #3	77A2-6Ib #5	76B1-107-AIIb	77A1-112II #1
Type	GC	GC	Flat	Flat	GC	Power Flat	GC	Flat	Power Flat	GC
Gate Width (μm)	600	600	600	600	1200	1200	1200	1200	1200	1200
Gate Length (μm)	~2	~2	~2	~2	~1	~1	~1	~1	~1	~1
Frequency/Bandwidth (GHz)	9.5	9.5	9.5	9.5	8.6	9.5	9.5	9.5	9.5	9.5
DC Bias (V)										
V_{GS} (V)	-1.5	-1.5	-1.5	-1.5	-1.09	-2.2	-3.0	-3.0	-2.0	-3.0
V_{DS} (V)	6.0	6.0	6.0	6.0	7.4	8.0	8.0	8.0	7.0	6.0
Input Power (dBm cw)	6-15*	6-15*	6-15*	6-15*	16-21	22	4-22†	4-22†	4-22†	15
1 dB Gain Compression (dBM)	16	15.8	12.6	13.4	21	21.9	-	21.6	18.8	-
AM/PM (°/dB)	1.0	1.2	3.7	3.2	-	-	-	-	-	-

* Tuned at 15 dBM

† H_2O cooled; tuned at 13 dBM

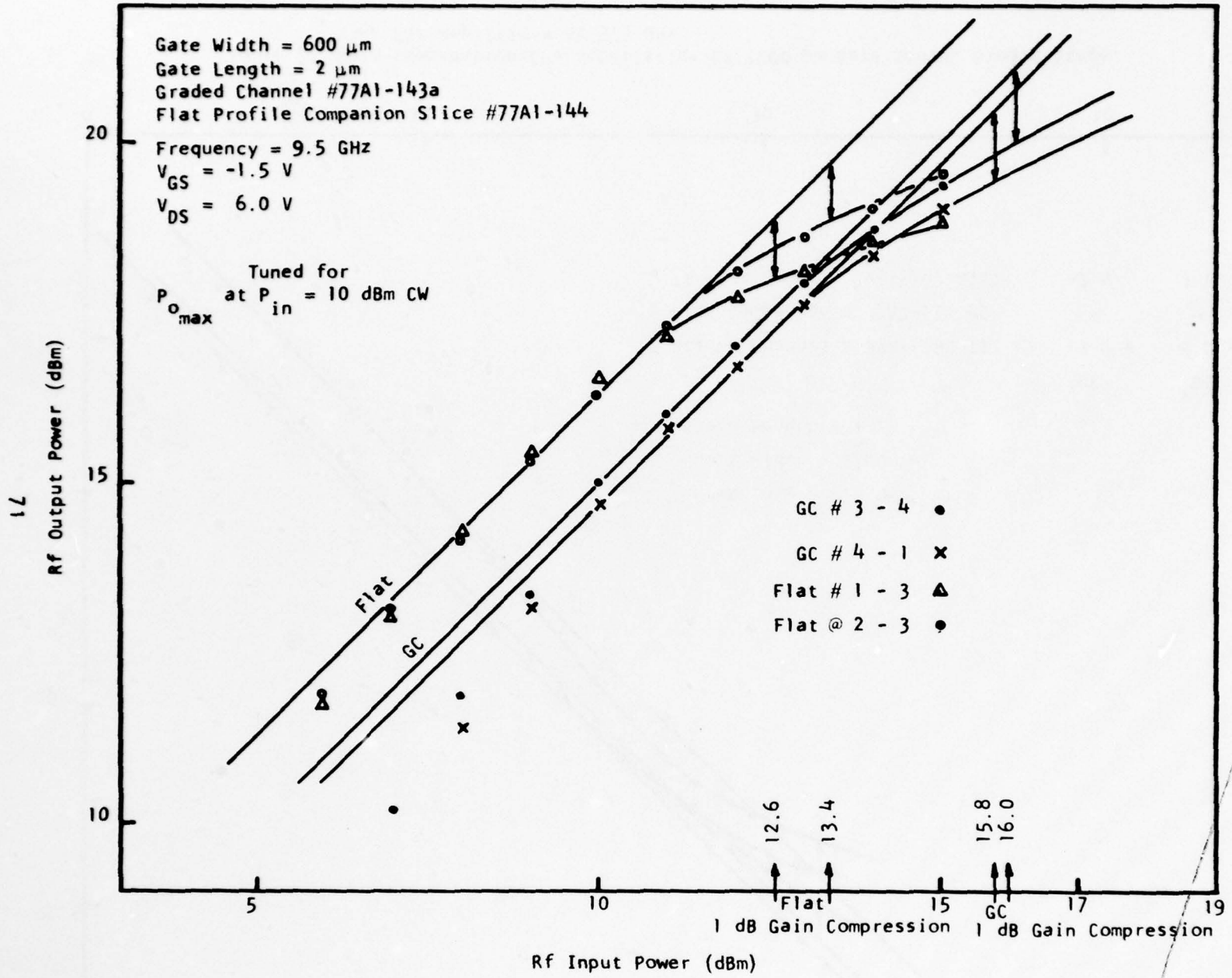


Figure 26 Gain-Compression Characteristics of 600 μm Gate Width Single-Stage GaAs FET Amplifiers at 9.5 GHz

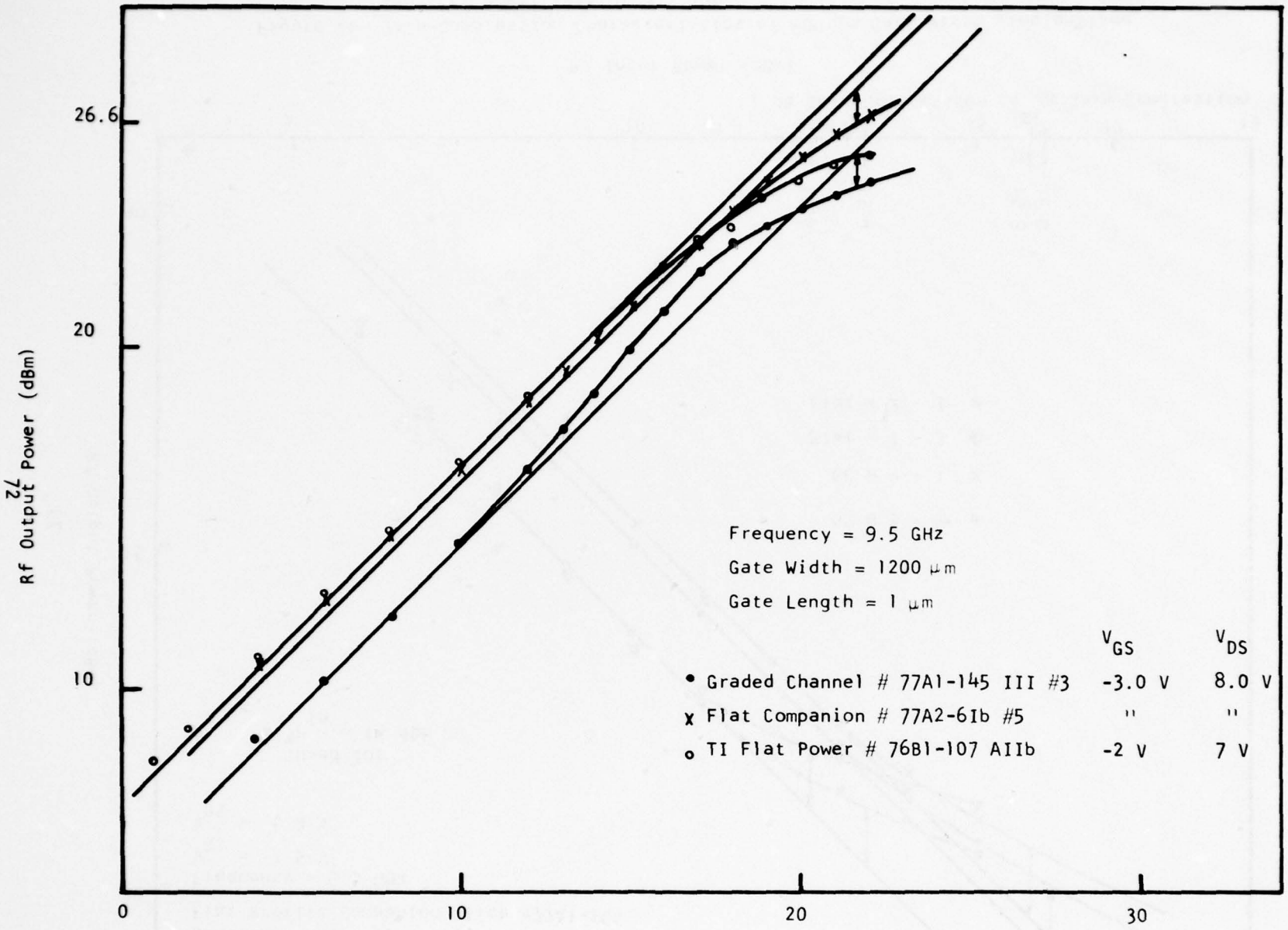


Figure 27 Gain-Compression Characteristics of 1200 μm Gate Width, Single-Stage GaAs FET Amplifiers at 9.5 GHz

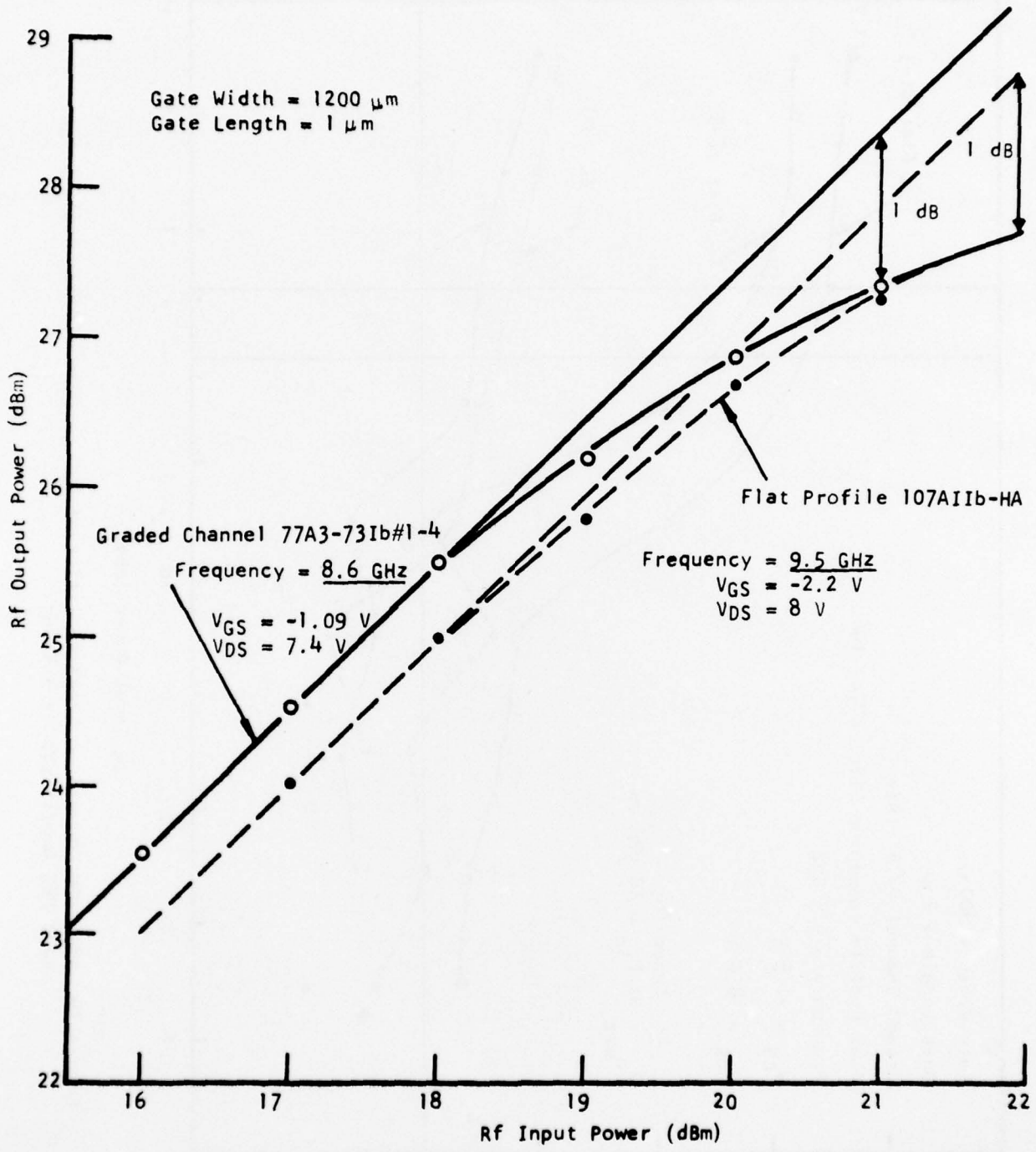


Figure 28 Gain Compression Characteristics of 1200 μm Gate Width Single-Stage GaAs FET Amplifiers at 8.6 GHz and 9.5 GHz

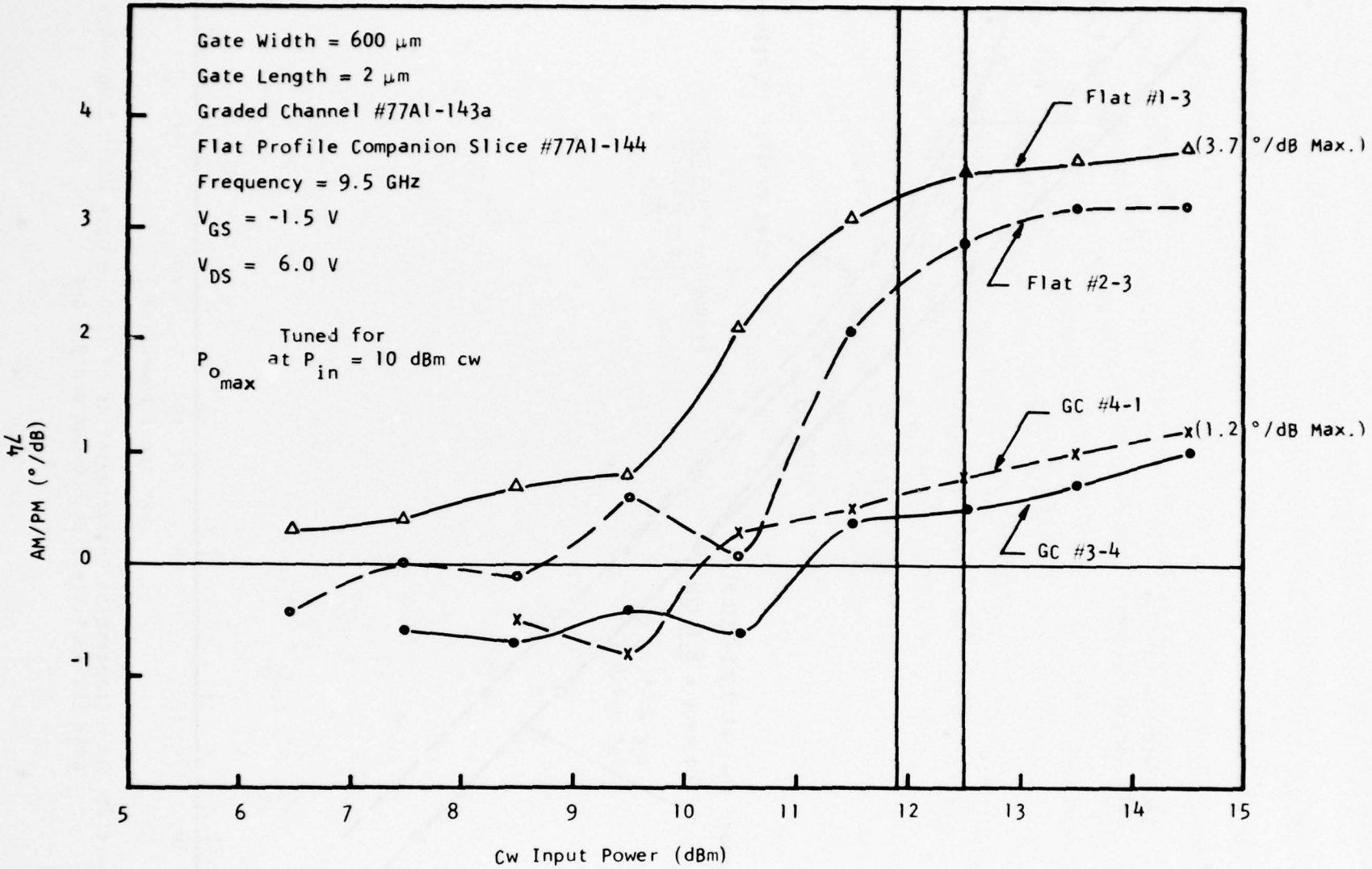


Figure 29 AM-to-PM Conversion Characteristics of 600 μm Gate Width, Single-Stage GaAs FET Amplifiers at 9.5 GHz

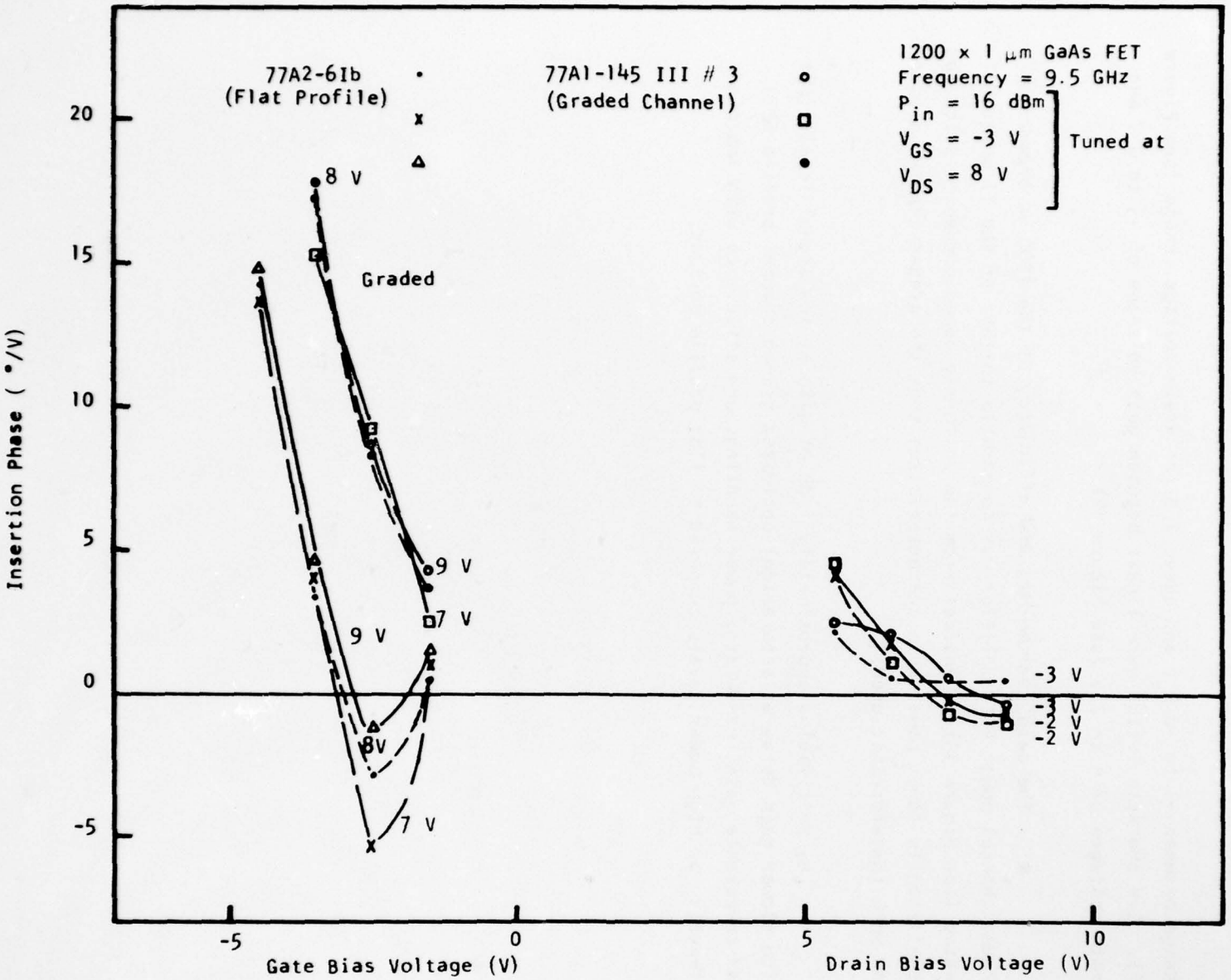


Figure 30 Insertion Phase Sensitivity to Variations in Bias Power Supply of 1200 μm Gate Width Graded Channel and Flat Companion Slice FETS

change between -3 to -0.5 V and above 7 V for drain voltage change (see Figure 31). I-V characteristics were linear between gate voltages of -3 to 0 V and drain voltages of 4 to 7 V (see Figure 32).

- The gain, bandwidth, and efficiency of the 1200 μm broadband graded channel power FET amplifier was comparable to that of the TI power FET tested (see Figure 33). [Devices from the uniformly doped companion slice had significantly lower power gain characteristics than the graded channel device and were therefore not used.]

By sacrificing approximately 1 dB of gain at low signal levels (but with slower gain decay at saturation) optimized graded channel profile FETs had comparable gain, bandwidth, power handling, and efficiency with improved linearity at high power levels compared to flat profile devices.

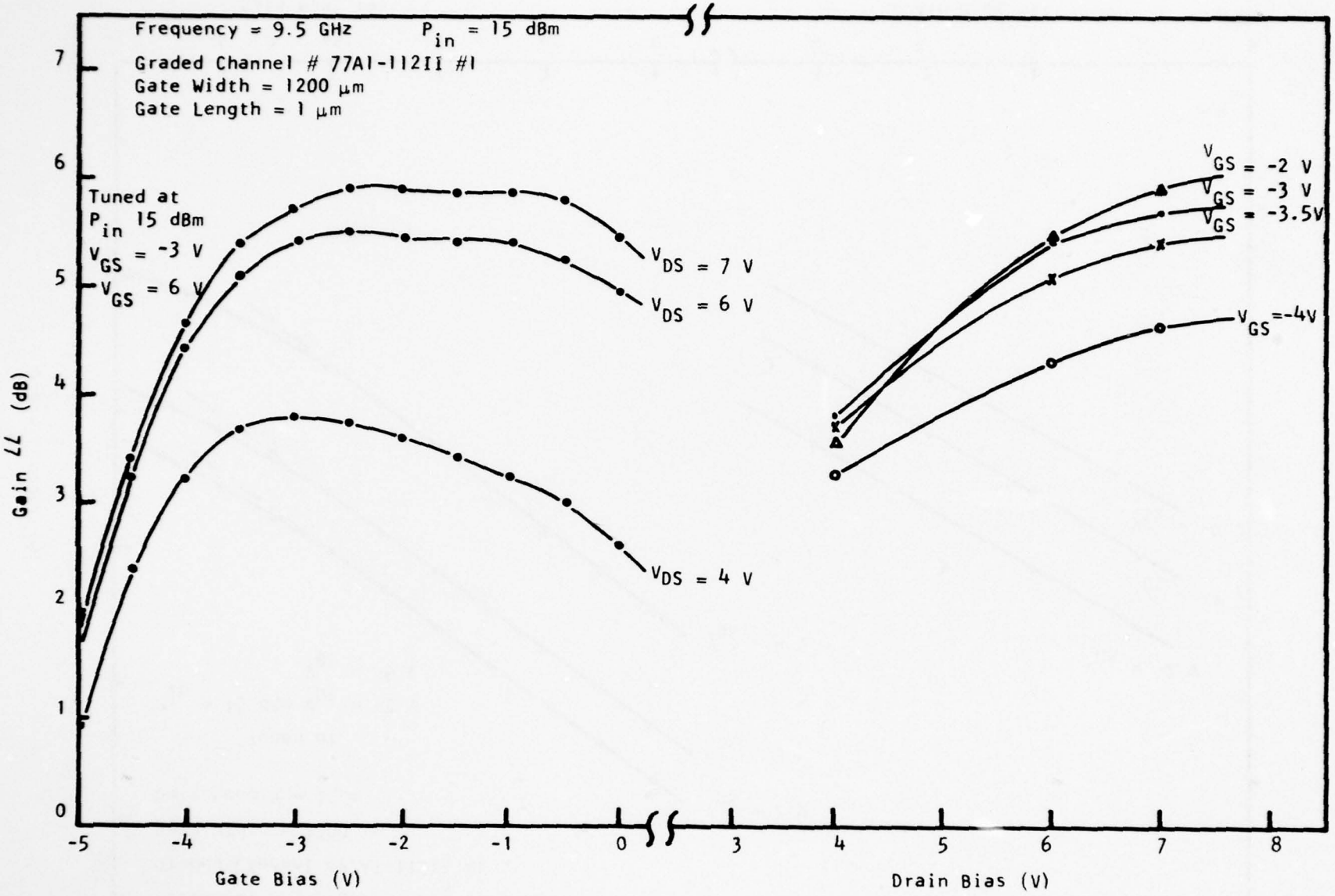


Figure 31 Power Gain Sensitivity to Variations in Bias Power Supply of 1200 μm Gate Width Graded Channel FET

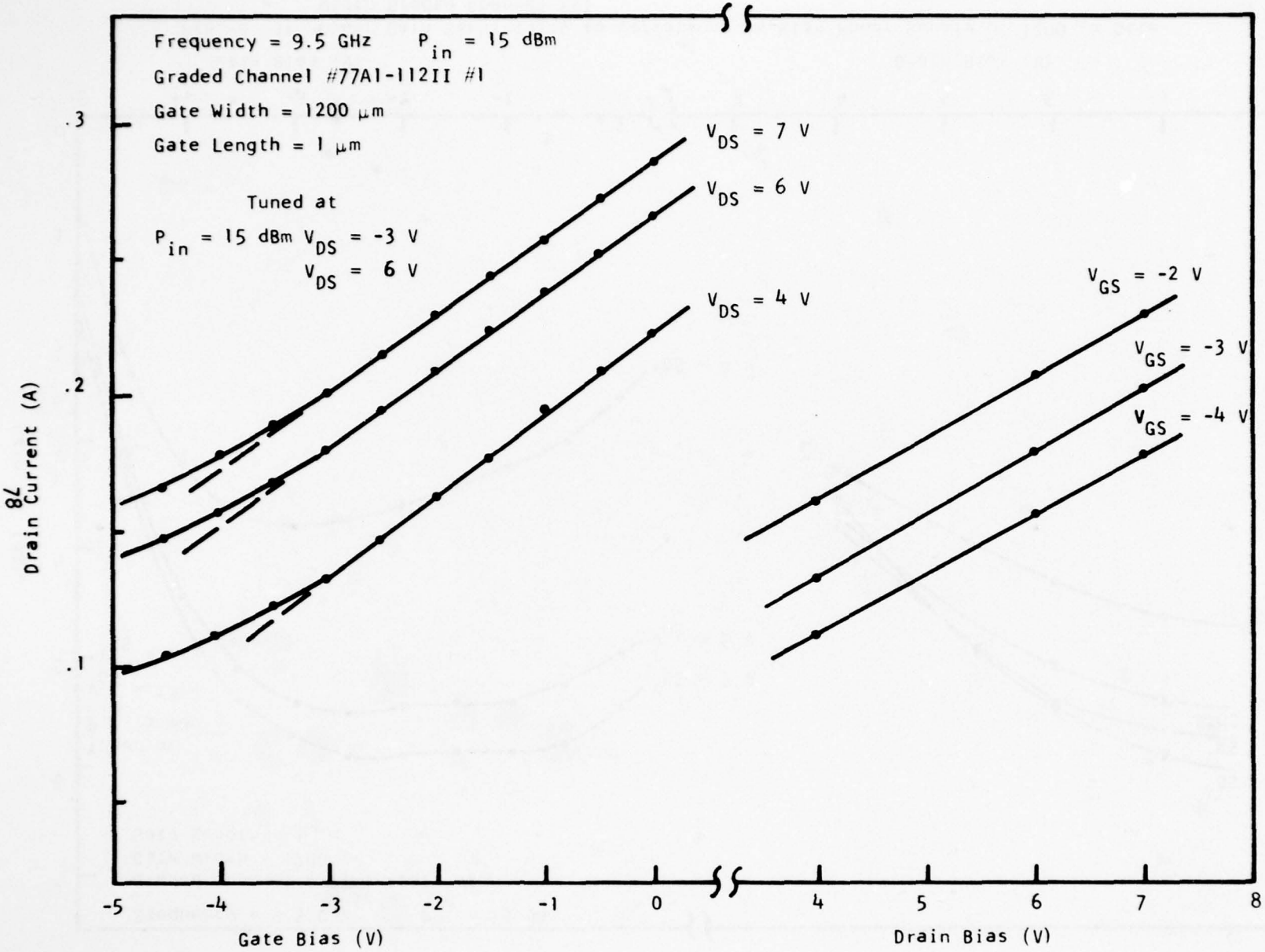


Figure 32 Drain Current Sensitivity to Variations in Bias Power Supply of 1200 μm Gate Width, Graded Channel FET

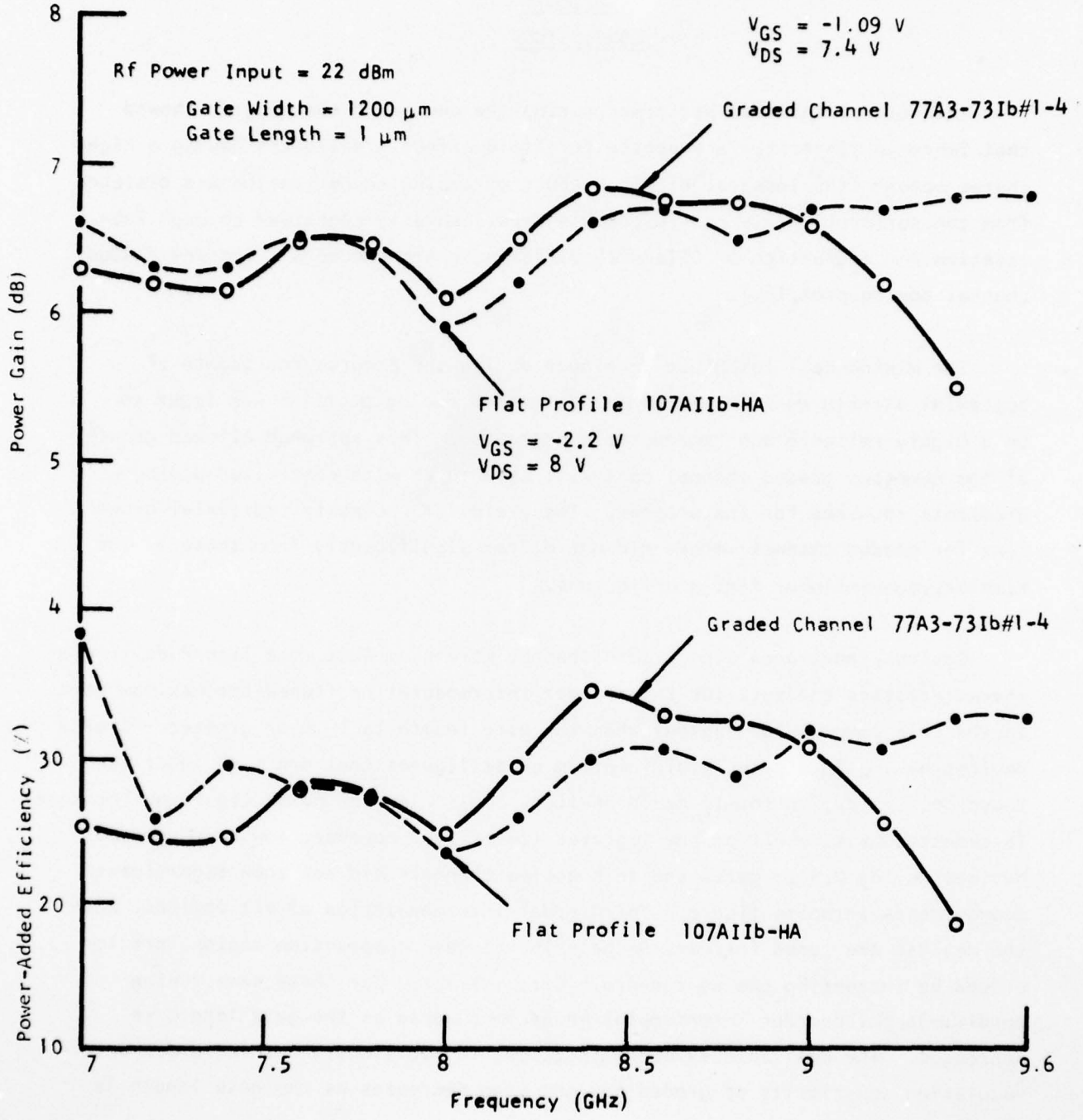


Figure 33 Power Gain and Efficiency of 1200 μm Gate Width Broadband GaAs FET Amplifiers as a Function of Frequencies

SECTION V
CONCLUSIONS

Theoretical analyses performed during the course of the program showed that improved linearity is expected for field effect transistors having a high charge moment (the integral of the product of doping concentration and distance from the surface). This conclusion was experimentally confirmed through fabrication and evaluation of FETs with differing charge moments (flat and graded channel doping profiles).

The mixing cell technique developed during the program for growth of epitaxial structures with exponentially graded doping profiles was found to be a highly reliable and reproducible procedure. This approach allowed growth of the numerous graded channel epitaxial structures with controlled doping gradients required for the program. The yields of successful epitaxial growth runs for graded channel wafers did not differ significantly from those of the simpler, conventional flat profile runs.

Devices fabricated from graded channel wafers exhibit more linear dc tranfer characteristics and superior third-order intermodulation (tuned for maximum gain in the gain compression region) when the gate length is 1 μm or greater. Graded devices having 2 μm gates yield minimum noise figures that are 1 dB lower than those of similar, uniformly doped devices. This superior noise figure performance is expected as a result of the improved linearity. However, low noise graded devices having 0.5 μm gates and thin active channels did not show significant improvements in noise figure. Third-order intermodulation of all devices, when the devices are tuned for maximum gain in the gain compression region, are improved by increasing the source-drain bias voltage. For these same tuning conditions third-order intermodulation becomes worse as the gate length is decreased. The available evidence suggests, in addition, the third-order intermodulation superiority of graded devices also decreases as the gate length is decreased below 1 μm.

When utilized in wideband amplifiers, 1 to 2 μm graded devices have gain, bandwidth, power, and efficiency comparable to those of flat profile devices and exhibit superior linearity and AM-to-PM conversion.

With appropriate modifications it is possible to use the self-limiting anodic oxidation thinning technique in a localized manner on slices having an epitaxial n^+ contact layer. It is therefore possible to anodically thin only the channel region, leaving n^+ material in the source and drain regions. Devices fabricated by this technique have source-drain burnout voltages that are 10 V higher than those of comparison devices that lack the n^+ contact.

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APPENDIX

PUBLICATIONS AND PRESENTATIONS

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The following papers were published for which credit was given under Contract No. N00014-76-C-1016:

R. E. Williams and D. W. Shaw, "GaAs FETs with Graded Channel Doping Profiles," Electron. Lett. 13, 408 (1977).

R. E. Williams and D. W. Shaw, "Graded Channel FETs: Improved Linearity and Noise Figure," IEEE Trans. Electron Devices ED-25, 600 (1978).

Corresponding talks, with the same titles, were given at the February 1977 (New Orleans) and February 1978 (San Francisco) meetings, respectively, of the Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD).